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Fabrication of Double Gate FET and Analytical Modeling for Surface Potential and Short Channel Effects

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Abstract: This paper explores the solution of surface potential variations for junction less (JL) double gate FET. This was only possible for SOI FET. Drain current and gate to source voltage V_{gs} characteristics within drain induced barrier lowering (DIBL) and Sub threshold calculations are done using Silvaco TCAD software. Basically In this paper 80nm device is fabricated and then some results are compare with device of 10nm.This is predominantly accurate for technical considerations of awareness where testified doping densities surpass 10 $cm^2$for 11nm to 21nm channel thickness.

Keywords: FET, DIBL (drain induced barrier lowering), TCAD, JL

1. INTRODUCTION

A recent perception of junction less field effect transistor within tri gate is presented here (Lee, *et. al,* 2009) and corroborated in (Lee, *et. al,* 2010). Likewise other architectures have also suggested in (Pfitzner, *et. al,* 2009) and (Weis, *et. al,* 2008) which is called vertical slit field effect transistor? The main difference in double gate FET is that current is carried by only majority charge carriers. Junction less topologies has many advantages (Lee, *et. al,* 2009), (Lee, *et. al,* 2010), (Pfitzner, *et. al,* 2009) such as deficiency of immediate junctions can be controlled at micro scales. It was observe that double gate devices shows better channel properties and DIBL in Accumulation mode (AM).On the other hand FETs having multigates do not have better effects (Weis, *et. al,* 2008). On current to off current ratios and SS (sub threshold slope) are generated (Lee, *et. al,* 2009). So we depend upon FET that is charge based (Sallese, *et. al,* 2005), (A Ali, *et. al,* 2016). Basically methodical model depends upon following two assumptions. a) semiconductor nano wire which is highly un dopped.b)statistics of Boltzmann (Jimenez, *et. al,* 2004), (Jamenez, *et. al,* 2004), (Jamenez, *et. al,* 2005), (Yu, *et. al,* 2007), (Kolberg, *et. al,* 2008), (Zhang, *et. al,* 2010) and (Vishvakarma, *et. al,* 2010). In 1990 characteristics of SOI MOSFET based on accumulation mode (AM) have presented (Colinge, *et. al,* 1990). Some limitations are shown by this model, which make this impracticable for doping concentrations and existing day geometries.

1. Substrate is supposed to be equipotential so between the BOX and vertebral connection no voltage drop occurs.

2. Most important feature of FETs which is sub threshold it's not mention.

3. In Poisson's equation sudden depletion calculation is consider. i.e inside the channel unbiased region is continuously occurring.

4. In additionally at the subordinate body surface induced by a adverse substrate biased is flout.

This paper propose theoretical model of junction less FET without any of the above-mentioned limitations. The initial point is a difficult strength of the relationship between the voltage of gate and surface potential. When device functions in depletion a better approximation is given in detailed in (Gnani, *et. al,* 2011, Ali, *et al.* 2018). Simulations are done on silvaco TCAD section II describes the fabrication of device .section III define the poisson equation and further its soluions are explain too. In section IV short channels description is explain. and similarly description of models for current and surface potentials with details are given. Calculations of DIBL and SS (subthreshold slope) are presented here.

2. DISCRIPTION OF DEVICE

Consider junction less double gate filed effect transistor as shown in figure1 with a silicon body n+ doping. t_{ox} is presenting the oxidation thickness of both gates which are located at the top and bottom position of the body. Drain and source are located at inside. A methodical solution for the potential surface is done here that eliminates the some limitations. We may explain the voltage difference:

$$V_g - V_b = \phi_{GB} + \Delta\phi_{SB} + \Delta\phi_{BX} + \Delta\phi_{SUB}$$

In the above equation

$$\phi_{GB} \approx \frac{E_g}{2q} - \phi_{Th} \ln\frac{N_A}{n_i}$$

It is the work function of gate.

Thermal voltage of device can be written as;

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$$\emptyset_{Th} = \frac{K_B T}{q}$$

And voltage drop, substrate. Body of the silicon, back oxide through the gate oxide can be define as

$$\Delta\emptyset_{Ox}, \Delta\emptyset_{Sub}, \Delta\emptyset_{sb}, \Delta\emptyset_{bx}$$

Then

$$\Delta\emptyset_{sb} = \emptyset_s - \emptyset_b$$

Here

$\emptyset_J$ = lower surface potential

$\emptyset_s$ = upper surface potential

From the above equation we can conclude that constant Fermi potential is presented within a semiconductor material.

Fabrication of DG FET is simulated in silvaco TCAD as shown below:

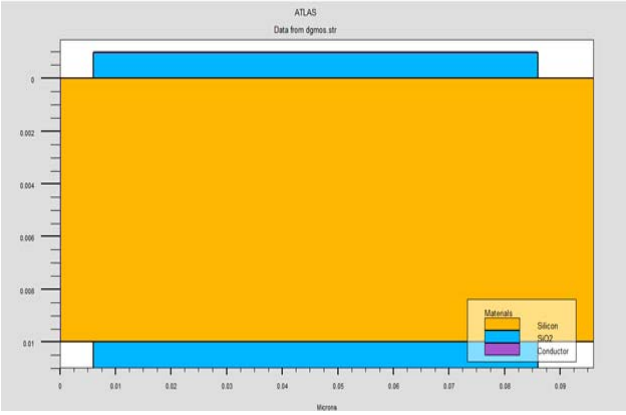

Fig-1 Fabrication of junction less double gate FET on Silvaco TCAD

3. POISSION EQUATION

In thermal balance conditions the Fermi level of potential where $F = F_B$ is constant. For this purpose we select x axis in the upper oriented direction so this equation can be standardized as:

$$\frac{d^2u}{dx^2} = -\frac{1}{\lambda_{sub}^2}\{[\exp[-(u-u_B)-1] - (\frac{n_i^2}{N_A^2})[\exp(u-u_B-1)$$

In above equation

$$u = \frac{\phi}{\phi_{Th}}$$

$$u_B = u_B - \ln\frac{N_A}{n_i}$$

$$\lambda_{sub} = \sqrt{\frac{\varepsilon_s \phi_{Th}}{qN_A}}$$

Then

$$u' = (u = u_B) = 0, u(x = -t_{bx}) = u_{ss}$$

In this equation

u_{ss} = substrate surface potential

$$= \pm\frac{\sqrt{2}}{\lambda_{sub}}\{[\exp(u_B - u) + (u - u_B) - 1] + (\frac{n_i}{N_A})^2(\exp(u - u_B) - (u - u_B) - 1)\}$$

$$= \pm\frac{\sqrt{2}}{\lambda_{sub}}F_{sub}(u, u_B)$$

$$\pm = (u_{ss} - u_B)/|u_{ss} - u_B|$$

Charge density can be found as;

$$Q_{ss} = -\varepsilon_s\phi_{Th}u'(u_{ss}) = \pm\sqrt{2}C_{sub}^{nor}F_{sub}(u_{ss}, u_B)$$

Now applying the boundary conditions:

$$u_B = u_{ss} - (Q_{ss} + Q_{bxe} + Q_{it})/(\phi_{Th}, C_{ox})$$

$$Q_{bxe} = \int_0^{t_{bx}} \rho_{bx}(x)\left(1 - \frac{x}{t_{bx}}\right)dx$$

4. SHORT CHANNEL EFFECT

Minimum surface potential is measure for calculating reverse charge, Using Gausses law

$$-\xi(x)\frac{t_{si}}{2} + \xi(x+dx)\frac{t_{si}}{2} - \xi_s(x)\,dx = -\frac{qN_A t_{si}}{2\,\varepsilon_{si}}$$

Electric field $\xi(x)$ can be calculated as:

$$\xi(x) \approx \frac{1}{\eta}\frac{d\psi_s(x)}{dx}$$

In This equation η is fitting parameter that integrates the consequence of the variation of the adjacent field in the depleted film. For surface potential following equation presents the surface potential.

$$\frac{d^2\psi_s}{dx^2} - \frac{2\eta C_{ox}}{\varepsilon_{si}t_{si}}\psi_s = \frac{\eta}{\varepsilon_{si}t_{si}}[qN_A t_{si} - 2C_{ox}(V_{GS} - V_{FB} - \phi_{Fi})]$$

Solution Of the equation can be explained as:

$$\psi_s(x) = C_1\exp(m_1 x) + C_2\exp(-m_1 x) - \frac{R}{m_1^2}$$

C_1 and C_2 are coefficients

$$C_1 = \frac{\phi_s[1 - \exp(-m_1 L)] + V_{ds} + R(1 - \exp(-m_1 L)}{2\sinh(m_1 L)}$$

$$R = \eta\frac{qN_A t_{si} - 2C_{ox}(V_G - V_{FB} - \phi_F)}{\varepsilon_{si}t_{si}}$$

$$m_1 = \sqrt{\frac{2\eta C_{ox}}{\varepsilon_{si}t_{si}}}, \phi_s = \left(\frac{kT}{q}\right)\ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Position in channel can be found as

$$x_m = \frac{1}{2m_1}\ln\left(\frac{C_2}{C_1}\right)$$

Now we can derive relationship for $\psi_s(x_m)$

$$\psi_s(x_m) = 2\sqrt{C_1 C_2} - \frac{R}{m_1^2}$$

5. SUBTHRESHHOLD SWING

Sub threshold can be define as it is characteristic of FET's voltage and current .In this region drain current is

controlled by gate. Which is similar to as when exponential current increases for forward biased diode.so swing which is produce during this region that is called subtheshold swing. Formula for calculating sub threshold swing is;

$$S = \frac{dV_g}{d(\log I_D)} \frac{mV}{dec}$$

We can control sub threshold by diffusion current then this sub threshold voltage can be limit. For an ideal device minimum sub threshold swing is:

$$S_{MOSFET} = \ln(10) \frac{kT}{q} \frac{mV}{dec}$$

It is $60 \frac{mV}{dec}$ at the room temperature ($300K$)

6. APPROACH OF MODELING

Main Approach is 2D closed form Poisson equation solution $\varphi_{poisson}$ in the area of channel (Schwartz, *et. al,* 2012). For considering parabolically shaped potential at source and drain sides to channel, and supplementary 2D secure form parabolic elucidation φ_{para} from (Kloes, *et. al,* 2008, (Ahmed, *et al*. 2018, Ali, *et al,*. 2017). It was instigated for region of channel. Mock 2D potential lean-to for drain and source, ϕ_{ext} is based upon operative build in voltage (Kloes, *et. al,* 2008), (Graef, *et. al,* 2013, Ali, *et al.* 2016).

7. CURRENT MODEL

Drain current can be designated following the indication of Pao And Shah (Pao, *et. al,* 1916) which comprises the diffusion transport predispositions and drift that is operating between the saturation and linear regions (Ortiz-Conde, *et. al,* 2007), (Song, *et. al,* 2009).
Drain current can be written as;

$$I_D = w \frac{W}{L} \int_0^{V_{DS}} Q_i dV$$

Q_i is the charge ,which can be explain as

$$Q_i = -2q \int_0^{\frac{t_{si}}{2}} (n - n_i) dx$$

$$= -2q \int_{\psi_b}^{\psi_s} \frac{n - n_i}{F} d\psi$$

$$I_s = w \frac{W}{L} \frac{\mu_{si}}{t_{si}} \left(\frac{KT}{q}\right)^2 [\rho(\beta_d - \rho(\beta_s)]$$

Using silvaco TCAD graph between drain current via V_{GS} is shown below:

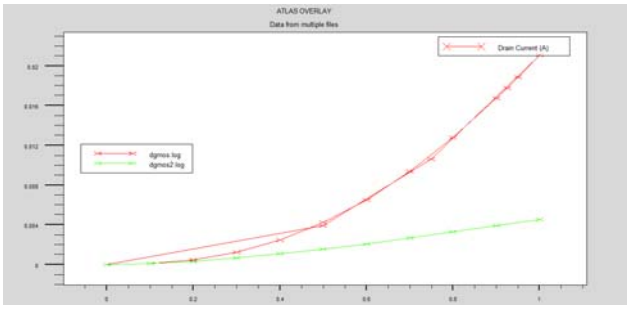

Fig-2 Current voltage characteristics of junctions less FET L=80nm, on silvaco TCAD

As shown in above figure drain current increases within the gate to source voltage .when $V_{GS} = 1V$ then amount of current is 0.02.Threshold is varying from 0.001V to 0.5V. When this voltage reaches to 0.12V, the current starts to go in saturation.

8. SURFACE POTENTIAL BASED MODEL

Two surface potential based models by Ortiz – conde et al and taur et al have been described Ortiz conde model monitored the double integral calculations of devices and bulk mass FET'S without some estimation.
Simulations for surface potential are shown below on TCAD.

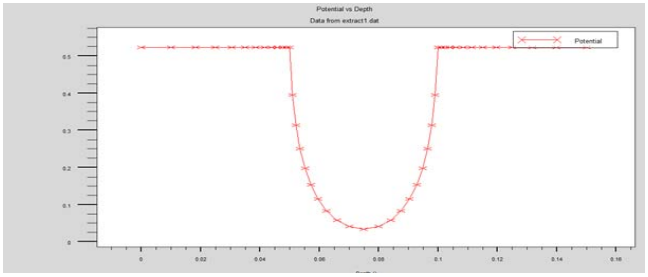

Fig-3 Plot of channel center position or surface potential via depth

Above plot presents the surface potential ψ_s and potential at the surface of channel ψ_0.calculated for voltage of gate is varying from 0 to 1.5 V in steps of 0.1v by varying the program for each step change. It is detect that below threshold semiconductor's charge gets minute. And volume inversion occurs in it.potential remains ($\psi_s = \psi_0$) through the whole silicon thickness .towards threshold voltage. Then voltage of gate increases in that result $\psi_s$rises slowly and ψ_0 does not consists on volume inversion.so the characteristics for device having different thickness but equal length through a single common point is called crossover point. **(Fig 4).** shows the potential variations at source to drain side that indicates that surface potential variations are different from this. So simulations had done on silvaco TCAD.

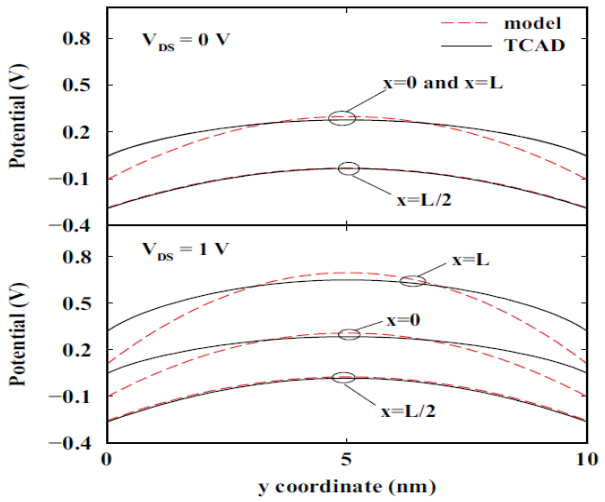

Fig-4 Plot of potential via length that indicates the variations of potential at source to drain edges

9. CHARGE BASED MODEL

In an intrinsic material there is no depletion region total charge is equal to inversion charge .so these characteristics will not be equal to surface potential

Simulations are done on TCAD:

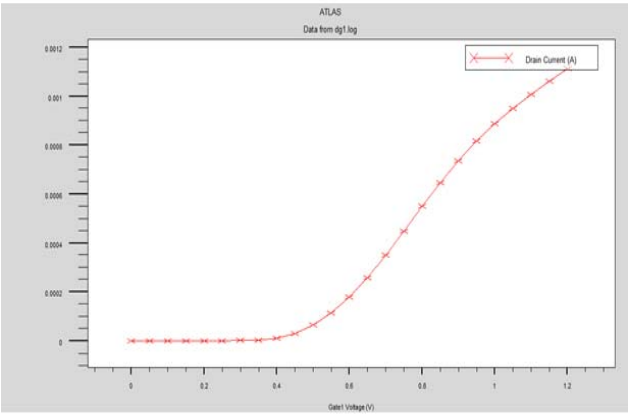

Fig-5 Drain current model based upon charge

Above simulation shows the horizontal translated $I_{ds} - V_{gs}$ characteristics for ($V_{ds} = 0.050V$) and $V_{gs} = 1.51V$.this transformation is called as DIBL which is categorized by the sum of millivolts of transformation per volt of variation in drain voltage.

Formula for calculating DIBL is

$$DIBL = \frac{V_T(V_{DSL}) - V_T(V_{DSH})}{V_{DSH} - V_{DSL}}$$

For the above case DIBL is equal to 63.580$\frac{mV}{V}$

Which is satisfactory because for a well-designed FET DIBL should be less than $\frac{100mV}{V}$

This figure presents the subthreshold slope too.it can be calculated form the above mention plot be for this we must have to know about formula that can be define as:

$$SS = \frac{\Delta V_{GS}}{\Delta \log_{10}(I)}$$

Basically

It is the sum of millivolts of rise in voltage of gate to require to rise the current of gate by the aspect of 10.00.Maximum limitation of sub threshold at room temperature is $\frac{60mV}{decade}$

Well design FET can tolerate sub threshold slope less than $\frac{80m\,V}{V}$.For above plot sub threshold is $72.6\frac{mV}{decade}$

10. CONCLUSION

This paper investigates the threshold voltage and surface potential variations, in junction less double gate FET'S, and solutions of poisson equation. Simulations are done on silvaco TCAD and some results have compared.

Similarly solutions of DIBL (Drain induced Barrier lowering) and SS(sub threshold slopes).effect of short channels are explained. Doping concentration for $N_D = 1 \times 10^{18} cm^{-3}$ indicates the DIBL $63.580\ \frac{mV}{V}$ and sub threshold slope is $72.6\frac{mV}{decade}$.

It can be predicted that upcoming developments of junction less FET'S will powerfully focused on this direction.

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