



FPGA Based Control Strategy for Three phase DC-DC converter

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Abstract: This paper presents control strategy based on FPGA for three phase DC-DC converter proposed for high power applications. FPGA has been used to generate control signals for proposed converter. High frequency transformers (HFTs) are design for the proposed converters, not only for the same but also for the mismatch turn ratios so that the effectiveness of the control strategy be confirmed. Three inductor currents have the same average value so that the power balance sharing can be achieved, regardless of the imperfect turn ratios of HFTs. Finally, the experiment results are presented in the paper and are found satisfactory.

Keyword: DC-DC converter, High frequency transformer (HFT), Interleaving pulse width modulation (PWM).

1. INTRODUCTION

Three phase DC-DC converters permit sharing of current among phases, it is helpful in self-cancellation of high frequency components that are generated during operation of power electronic devices. Three phase DC-DC converters are used frequently in low-voltage, high power applications, due to similarity with conventional inverters in circuit configuration. These converters have gathered more engrossment of engineers and researchers nowadays. In practice not only three phase DC-DC converters but also six phase DC-DC converters are used. Multiphase configuration is used in order to increase the power rating of converter by increasing the phases of converter. Such converter avoids the circulating currents of transformers that is why they are most suitable for applications like fuel cell (Seung *et al.*, 2007) and have ability of high conversion ratios of voltage and currents (EG and G Technical Services, 2004). (US DOE National Energy Technology Laboratory, 2005)

Three phase converters can be operated at increased power levels because of current sharing properties (Wong, *et al.*, 2005) (Balogh, 2005) (Mao, *et al.*, 2006). Proper current sharing is required to make certain that converters share current to their capacity and maintain stability. Usually currents of individual phases in three phase DC-DC converters are equally divided (Juanjuan, *et al.*, 2006) Imperfect matching in phase currents can make the converters overloaded and lead them and reduce its operating performance and efficiency (Qahouq, *et al.*, 2002) (Panov *et al.*, 2001), but not to worry there is alternatives available if currents are not

divided properly as (Peterchev, *et al.*, 2003). Nowadays, the applications where compact size, high efficiency and low EMI emission is required three phase DC-DC converters are proposed (Seung *et al.*, 2007) (Waffler, *et al.*, 2007), (Eckardt, *et al.*, 2006). Efficiency of three phase converter can more be increased by using modern switching techniques as soft switching and use of power electronic switching devices like that are made of silicon carbide material.

Three phase DC-DC converter consisting of boost half bridge (BHB) cells and a control strategy based on FPGA are proposed for high-power applications in this paper. Generalized three phase DC-DC converter is configured to increase the output power; therefore BHB cell and voltage rectifier are connected in parallel at primary and secondary side of HFTs respectively. Furthermore, FPGA has been used to generate the control signals for switches used in the proposed three phase converter topology. In order to check effectiveness of the control strategy, the proposed three phase converter has been configured for the same and/or mismatch turn ratios of HFTs.

2. SYSTEM DESCRIPTION AND CONTROL STRATEGY:

Fig.1 shows proposed circuit of three phase DC-DC converter. Proposed DC-DC converter consisting of three high frequency transformers (HFTs). Primary side of each HFT is connected to DC supply voltage along with an inductor and half bridge inverter. Whereas secondary side of each HFT is connected to parallel rectifier and load resistor. The turn ratios of the HFTs

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can either be the same or mismatch. In this paper the turn ratios of HFTs are purposely made mismatched in order to verify the effectiveness and stable operation of the system.

The interleaving PWM technique has been used for proposed three phase converter. The interleaved PWM switching is shown in (Fig. 2) which is used as driving signals for the switches and is generated by FPGA. Each leg of the BHB cells has a phase difference of 120° . The device current rating can be reduced by increasing the number of BHB cells on primary sides and voltage rectifiers on the secondary sides of HFTs. Suppose N voltage rectifiers are connected in parallel, then the phase shift of each leg will be $2\pi/N$. The driving signal is generated by FPGA CycloneII EP2C8Q208C8N. Using FPGA as a controller has advantages: it contains more than 200 I/O pins which give provision of controlling circuits with many switches, it can work on high frequency and high speed in order to reduce the size of the circuit and increase the power density, it is user friendly for programming etc.

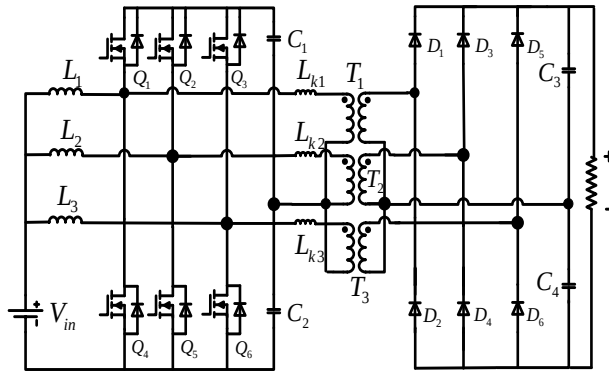


Fig. 1 Proposed Three phase DC-DC Converter

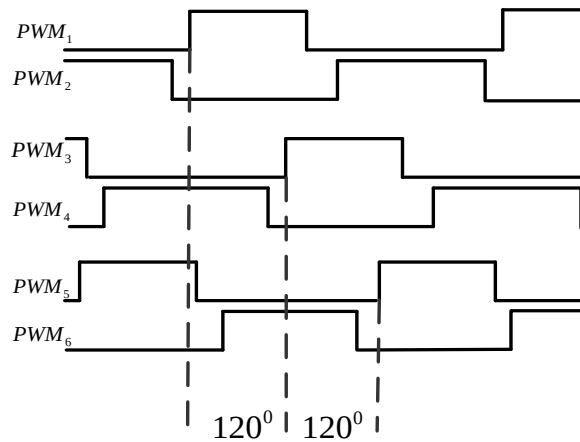


Fig. 2 Interleaved PWM Switching

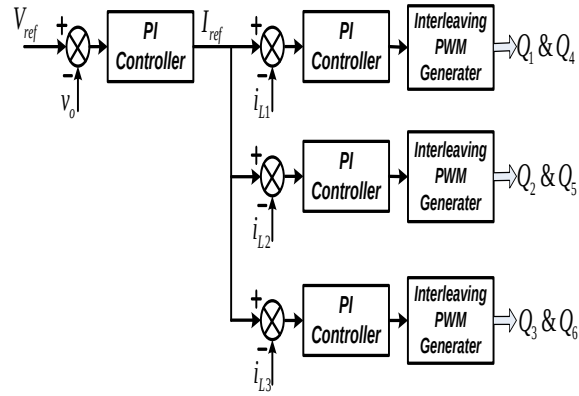


Fig. 3 Proposed Control strategy

In order to obtain power sharing balance especially when the turns ratio are mismatched, the control loop for the proposed circuit contains one voltage loop and three input current loops. As shown in (Fig. 3), the voltage loop senses the output voltage of the load V_o , comparing with reference voltage V_{REF} , the result is calculated through a voltage loop PI regulator in order to get a current reference value I_{REF} . The three current sensors in the current loops sense the input inductor currents of each BHB cell individually, to get each input inductor current I_{L1} , I_{L2} and I_{L3} . These three values are compared with I_{REF} , and then calculated through PI regulators of individual current loops so that the comparing values of each leg's PWM generators can be obtained. As the peak value is a constant, and the dead time between the upper and lower switches in each leg is determined, the driving signal for each leg of the converter can be generated using interleaving PWM technique.

3.

EXPERIMENTAL RESULTS

The control strategy has been verified by building a 2-kW laboratory prototype of proposed converter, and circuit parameters are in (Table 1). To decrease the volume of the input inductors and the high frequency transformers, the switching frequency for all six MOSFETs is 40 kHz, with Altra's FPGA CycloneII EP2C8Q208C8N as the controller. MOSFETs with low drain to source resistance and extremely high dV/dt capability are used. Schottky diodes with lower reverse recovery loss and forward voltage drop are used as voltage rectifiers. Experimental results are shown in (Fig. 4) for the same turn ratios and (Fig. 5) for the mismatch turn ratios of HFTs. (Fig. 4.1) represents the output voltage and input inductor currents at steady state condition. (Fig. 4.2 and Fig. 4.3) show the dynamic response, when increasing and decreasing the load. Similarly, Fig. 5 describes the same as mentioned above with mismatch turn ratios of HFTs.

Table. 1 Specification

Parameters	Value	Parameters	Value
P_O	2 kW	$L_1 \sim L_3$	500 μ H
V_O	200 V	C_1, C_2	47 μ f
V_{in}	48 V	f_s	40 kHz

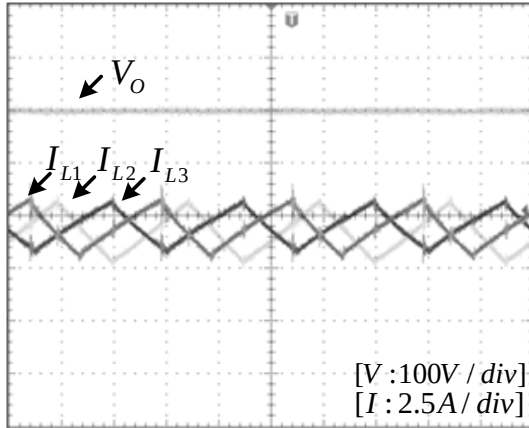


Fig. 4.1 output voltage and inductor currents

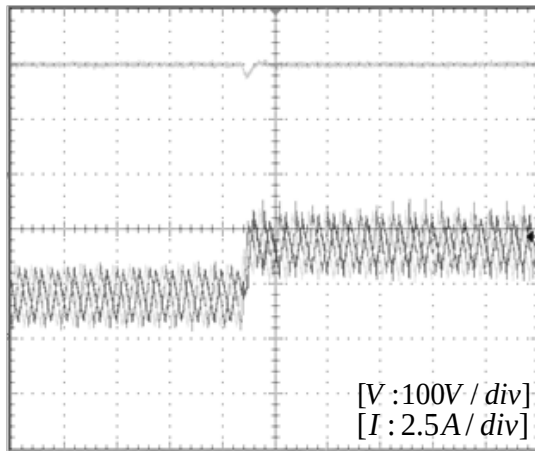


Fig. 4.2 Dynamic response for increasing load

[V : 100V / div]
[I : 2.5A / div]

Fig. 4.3 Dynamic response for decreasing load

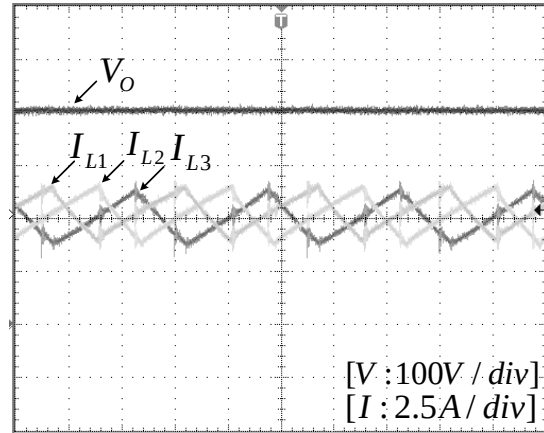


Fig. 5.1 output voltage and inductor currents

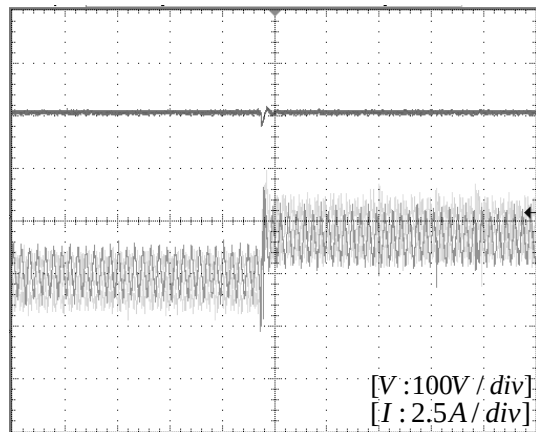


Fig. 5.2 Dynamic response for increasing load

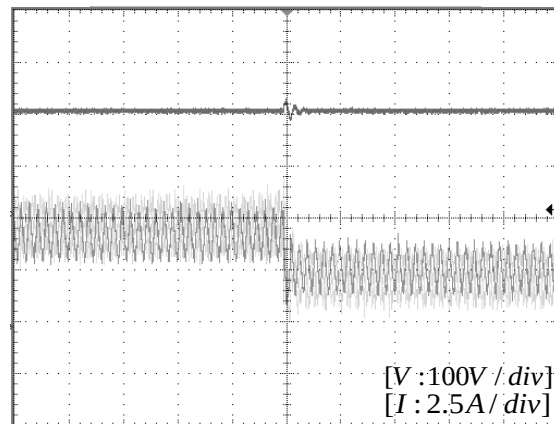


Fig. 5.3 Dynamic response for decreasing load

4.

CONCLUSION

Three phase DC-DC converter and a control strategy based on FPGA have been proposed in this paper. In the proposed three phase converter interleaving PWM technique has been applied. Based on experimental results it can be concluded that power balance sharing

can be obtained between input and output, no matter the turn ratios of HFTs are same or mismatched. Effective and stable results are found for the control strategy based on FPGA with good steady state and dynamic response of the system.

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