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Evaluation and Comparison of Small Signal AC Parameters of submicron GaAs FET from its Measured DC Characteristics with Lowest RMS Error

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Abstract: In this paper we discuss the comparison and evaluation of small signal AC parameters of GaAs Field Effect Transistor (FET) from its measured DC characteristics. For this purpose five different FET models i.e., Curtice, Materka, Statz, Ahmed and Noor, have been presented and their ability to simulate submicron GaAs FET's characteristics is checked by MATLAB.A technique is applied to estimate intrinsic small signal parameters of GaAs FET. In this technique DC characteristics of a device are first evaluated. The observed characteristics are then simulated by using two GaAs FET DC models which simulate the submicron GaAs FET's *I-V* Characteristics. Those models are Noor and Ahmed model. During AC parameters extraction process, once a good DC match is attained then by employing simulated I-V characteristics, intrinsic small signal parameters are evaluated for which a complete set of mathematical expressions has been discussed.

Keywords: GaAs MESFET, DC Models, AC Parameters

Index Terms: GaAs MESFET, DC Models, AC Parameters.

Nomenclature

(YES NOMENCLALUEE IS IN THE BIGGING OF MANUSCRIPT)

a	Epi-layer thickness
d	Interfacial layer thickness
g_d	Output conductance
g_m	Transconductance
I_g	Gate current
L_G	Gate length
N_d	Doping density of the channel
q	Electronic charge
V_d	Voltage drop
V_T	Threshold voltage
Φ_b	Schottky barrier height
R_s	Source resistance
R_g	Gate resistance
R_d	Drain resistance
R_i	Channel resistance
R_c	Contact resistance
L_s	Source inductance
L_g	Gate inductance
L_d	Drain inductance
C_{gs}	Gate-source capacitance
C_{gd}	Gate-drain capacitance
C_{ds}	Drain-source capacitance
C_{pg}	Gate-pad capacitance
C_{pd}	Drain-pad capacitance
f_τ	Unity gain frequency
τ	Trannsit time delay

1. INTRODUCTION

GaAsfield effect transistors (FETs) with short channel lengths can operate at a frequency greater than 100 GHz (Golio and Golio, 1991), (Das, 1987). The designing of an ac prober for assessing ac parameters of GaAs FETs at such a high frequency is an extremely difficult task. Usually, the frequency range is much lower than the maximum expected device response. And the device AC parameters under test are predicted by experimental extrapolation techniques (Enoki, *at el*, 1990), (Golio , 1990) .

An evaluation of FET DC characteristics is a straightforward process and evaluation of FET characteristics can be performed readily for both packed and unpacked devices (Memon, *at el*, 2009), (Iqbal, *at el*, 2005). Alternatively, an AC prober requires a very precise calibration for accurate AC parameter extraction. Thus, the process of extracting AC parameters by using AC proberis complex and can affect industrial throughput (Hwang. *at el*, 1989), (Debie and Martens, 1995). In 2009, a technique for assessing submicronGaAs FET's AC parameters by employing its DC characteristics had been proposed by Noor (Memon, *at el*, 2007). The technique proposed by Noor is valid for submicronGaAs FET's which offer a reasonably good Schottky barrier response and also for non-ideal Schottky response.

The validity of this technique was demonstrated by employing at different submicron GaAs FETs characteristics.

DC characteristics based AC parameter evaluation process employs a nonlinear DC model which simulates the output and the transfer characteristics of the device by employing an optimization algorithm. Once a good fit is attained, the model is then extended to predict AC response of the device. The technique thus reduces the discrepancy between observed and simulated data which may arise due to non-ideal Schottky barrier response and short channel effects.

2. MATERIALS AND METHODS

The equivalent circuit of a submicron GaAs FET is dependent upon the physical construction of the device (Memon, *at el,* 2009). **(Fig. 1)** shows the constructive view of a GaAs FET.

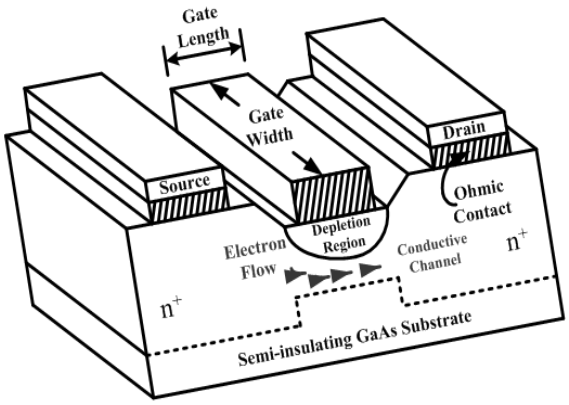

Fig. 1.Basic constructive view of a GaAs FET.

The origin of the device equivalent circuit elements is shown in **(Fig. 2).** The circuit elements shown in this figure are: Source resistance, *R*, Gate resistance, R_g, Drain resistance, R_d, Channel resistance, R_i, Contact resistance, R_c, Source inductance, L_s, Gate inductance, L_g, Drain inductance, L_d, Gate-source capacitance, C_{gs}, Gate-drain capacitance, C_{gd}, Drain-source capacitance, C_{ds}, Gate-pad capacitance, C_{pg} and Drain-pad capacitance, C_{pd}. The values of C_{pg} and $C_{pd}$are topology dependent and circuit topologies involving additional elements have been described in (Golio and Golio 1991). A complete common source AC equivalent circuit of a GaAs FET in the saturation region is shown in Fig. 3. In Fig. 3, circuit elements inside the box represent intrinsic elements of the device, whereas the other components are called extrinsic device components.

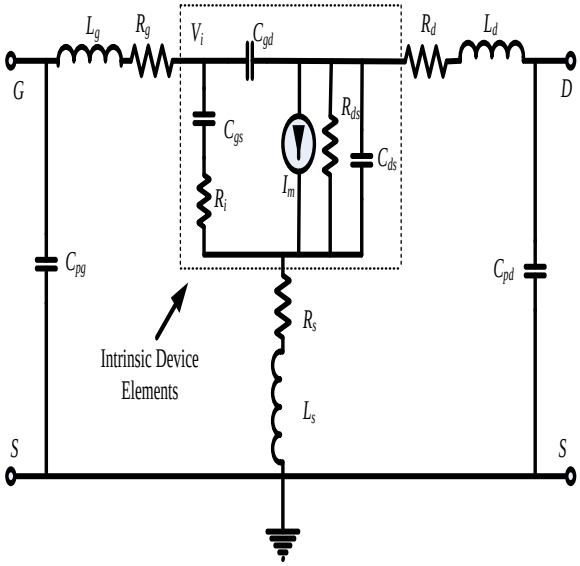

Fig. 2. FET's small signal equivalent circuits in to the saturation region of operation.

3. PROBLEM AND STATEMENT

GaAs FETs are, mainly, used in front-end amplifiers because of their best noise and high frequency properties. For establishing high frequency capabilities of GaAs FETs, AC equivalent circuit parameters are used. These AC small signal equivalent circuit parameters are controlled by the device fabrication and designing processes and assessed from its electrical response. For the extraction of these AC parameters two GaAs FET models which can simulate the submicron GaAs FET's *I-V* Characteristics i.e., Noor and Ahmed DC models. The mathematical expressions for these models respectively are (Memon, *at el,* 2007), ((Memon, *at el,* 1997).

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{(1+\eta\, e^{V_{gs}})(V_T + \Delta V_T + \gamma V_{ds})}\right)^2 \times \tanh(\alpha V_{ds})(1+\lambda V_{ds}) \quad (1)$$

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{(V_T + \Delta V_T + \gamma V_{ds})}\right)^2 \times \tanh(\alpha V_{ds})(1+\lambda V_{ds}) \quad (2)$$

Where

$$\Delta V_T = \frac{4a}{3L_g} V_T \quad (3)$$

(Fig.3 and Fig. 4) shows, the predicted and experimental*I-V* characteristics of a 0.2 x 200 μm^{2}GaAs FET by using Noor and Ahmed GaAs FET DC Model respectively.

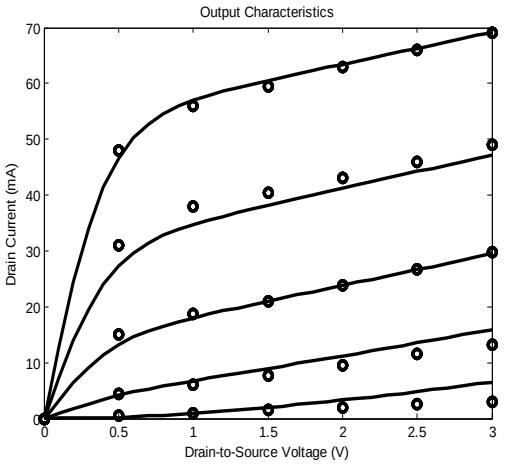

Fig.3.Experimental and predicted*I-V* characteristics of GaAs FET by using Noor Model.

RMS error values were calculated at different V_{gs} voltage for the Ahmed and Noor *I-V* models, as given in **(Table-1).** It has been observed that the RMS error of Noor model is comparably smaller than the RMS error of Ahmed model and these r GaAs FET models may be preferred for circuit designers with submicron GaAs FETs.

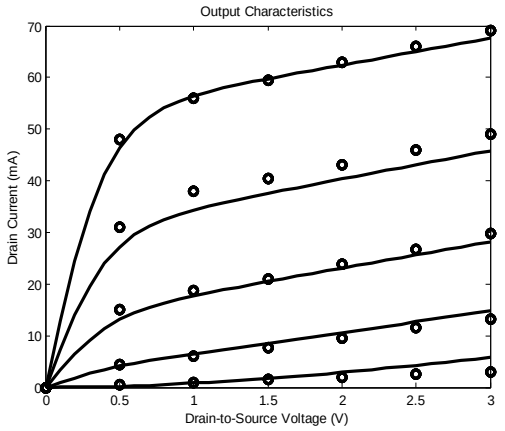

Fig. 4.Predicted and experimental *I-V* characteristics GaAs FET by using Ahmed Model.

Table-1. RMS errors of Noor and Ahmed GaAs FET model as a function of V_{gs}.

S. No.	Model	RMS error at different V_{gs}values					Av. Error
		-0.8	-0.6	-0.4	-0.2	0 V	
1.	Ahmed	0.56	0.45	0.52	0.93	0.85	0.66
2.	Noor	0.62	0.48	0.21	0.87	0.85	0.60

(Table-2) shows the expressions for AC parameters used in device modeling of GaAs FET. Where I_{ds}, are given in Equ.1 and Equ. 2 for Noor and Ahmed model respectively.

Table-2.AC Parameter Expressions for Device Modeling of GaAs FET

S. No.	Model Name	*I-V* Characteristics Expression
1	C_{gs}	$C_{gs} = \frac{q N_d v_s Z^2 \varepsilon_s L_G}{a q N v_s Z - I_{ds}}$
2	C_{gd}	$C_{gd} \approx \frac{\varepsilon_s \pi Z \sqrt{\Phi_b}}{2\sqrt{I_{ds}(V_{ds} - V_{gs} + \Phi_b) - I_{ds}^2 (R_d + R_s}}$
3	C_{ds}	$C_{ds} \approx \frac{2\pi \varepsilon_s Z I_{ds}}{L_G} \times \sqrt{\frac{2\varepsilon_s A}{q N_d}}$ where $A = \sqrt{\frac{(V_{ds} - V_{gs} + \Phi_b)}{I_{ds}} - (R_d + R_s)}$
4	g_d	$g_d = 3 \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right\|_{V_{gs}=const}$
5	$g_{m(ac)}$	$g_{m(ac)} = g_m e^{-j\omega\tau}$ Where $g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right\|_{V_{ds}=const}$
6	f_T	$f_T = \frac{1}{2\pi\tau}$
7	τ	$\tau \approx \frac{1}{2}\left[\frac{C_{gs} + C_{gd}}{g_{m(ac)}}\right]$
8	R_i	$R_i = \frac{1}{3}\left[\frac{v_s L_G}{\mu_e I_{ds}}\right]$

where I_{ds}, are given in Eq.1 and Eq. 2 for all expressions given in (Table-2)

4. SIMULATIONS

Gate-to-Source Capacitance, C_{gs}, is one of the important parameters which determines AC response of the GaAs FET and is usually known as Miller's capacitor (Iqbal, *at el*, 2005). The magnitude or value of C_{gs}capacitor can be assessed as (Memon, *at el*, 2009).

Equ.3 represent variation in C_{gs} as a function of V_{gs} and V_{ds}, where η is used to accommodate interface states. **(Fig. 5 and Fig. 6)** represent change in the magnitude of C_{gs} at various values of V_{gs} for both Noor and Ahmed model respectively. Investigation of these figures revealed that, by increasing the value of η the magnitude of C_{gs}capacitor also increases.

High value of η means a lesser component of applied V_{gs} is consumed in the modification of the gate

depletion, hence increasing in the value of C_{gs}. Although a higher value of C_{gs} capacitor limits the high frequency response of the device, which has not been taken into account in the model of Eq. (1). Thus, for the estimation of C_{gs} value by using this equation is confined to show a discrepancy in observed and simulated characteristics.

Similarly others AC parameters were also simulated the summary of these results is given in **(Table-3 and Table-4)** for Noor and Ahmed model respectively.

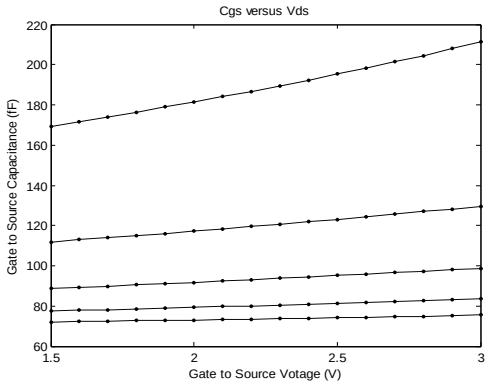

Fig. 5: Variation in Gate-to-Source capacitance as a function of V_{gs} for GaAs FET by using Noor Model.

5. RESULTS AND DISCUSSION

The device is biased to V_{ds} = 2 V and V_{gs} = - 0.4 V for the estimation of AC parameters. A reasonably good DC fit shown in **(Fig.4 and Fig. 5)** allows estimating AC parameters by using set of equations given Table-3. The evaluated AC parameters for Noor and Ahmed model are summarized in **(Table-3and Table-4)**. In these tables a comparison has been made between the observed and calculated AC parameters both by the technique.

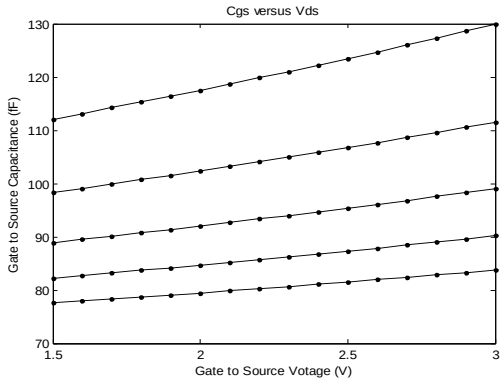

Fig.6: Variation in Gate-to-Source capacitance as a function of V_{gs} for GaAs FET by using Ahmed Model.

By examining the data available in the tables clearly shows that the technique is better and the values thus obtained are within acceptable experimental error margin and also the shows that Noor model is best for simulating the DC characteristics of submicron GaAs FET.

Table-3 Intrinsic equivalent circuit parameters of a 0.2 x 200 μm^{2}GaAs FET atVds = 2 V and Vgs = -0.4 V using Noor Model.

Elements	Experiment	Estimated Technique	Difference % Technique
C_{gs}(fF)	300	180	- 40
C_{gd}(fF)	20	18.5	- 7.5
C_{ds}(fF)	130	62	- 52.30
g_d(mS)	15	14	- 6.66
$g_{m(ac)}$(mS)	50	70	+ 40
τ (pS)	5	1.6	- 68
R_i(mΩ)	1	1.2	+ 20

Table-4Intrinsic equivalent circuit parameters of a 0.2 x 200 μm^{2}GaAs FET atVds = 2 V and Vgs = -0.4 V using Ahmed model.

Elements	Experiment	Estimated Technique	Difference % Technique
C_{gs}(fF)	300	160	- 47
C_{gd}(fF)	20	18	- 10
C_{ds}(fF)	130	60	- 54
g_d(mS)	15	7.5	- 50
$g_{m(ac)}$(mS)	50	80	+ 28.33
τ (pS)	5	1.5	- 70
R_i(mΩ)	1	1.25	+ 25

6. CONCLUSION

Here two FET models Ahmed and Noor have been presented and their ability to simulate submicron GaAs FET's characteristics is checked in MATLAB. To demonstrate the validity of a model, *I-V* characteristics of short channel FETs, are simulated and compared with experimental data. The accuracy of a model is reported by evaluating its RMS error values as a function of device biasing. It is noted that the Noor and Ahmed model, when applied to high frequency FETs, offers better simulation results compared to other models under consideration. A technique is applied to estimate intrinsic small signal parameters of GaAs FET for both models. In this technique DC characteristics of a device under consideration are first evaluated. The observed characteristics are then simulated by using the Noor and Ahmed model. The developed model has the capability to simulate *I-V* characteristics of GaAs FETs with varying Schottky barrier conditions. In general, it has been shown that the this estimation method is accurate as well as efficient in estimating AC parameters of GaAs FETs by using their DC characteristics, and could be employed as a useful tool in device simulation software.

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