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Comparison of GaAs FET Models for Simulating the I-*V* Characteristics Sub micron GaAs FET

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Abstract: The accuracy of a model is reported by evaluating its RMS error values as a function of device biasing. In this paper the comparison of five different FET models i.e. Curtice, Materka, Statz, Ahmed and Noor, have been presented, and their ability to simulate submicron GaAs FET's characteristics is checked by MATLAB. It is noted that the Noor model, when applied to high frequency FETs, offers better simulation results compared to other models under consideration. Whereas, the simulated results of Ahmed model are close to the Noor model. These models have been examined and discussed by considering the variables involved in their definition along with fitting parameters. To demonstrate the validity of a model, I-V characteristics of short channel FETs, are simulated and compared with experimental data.

Keywords: GaAs, MESFET, DC Models, RMS Error

Index Terms: GaAs MESFET, DC Models, RMS error,

Nomenclature

a	Epi-layer thickness
d	Interfacial layer thickness
g_d	Output conductance
g_m	Transconductance
I_g	Gate current
L_g	Gate length
N_d	Doping density of the channel
q	Electronic charge
V_d	Voltage drop
Φ_b	Schottky barrier height
Si	Silicon
Ge	Germanium
GaAs	Gallium Arsenide

1. INTRODUCTION

Transistors are the key active components of all modern utilities of electronics. Transistor is the incredible invention of 20th century (Price, 2004). A transistor is a three terminal semiconductor device used to amplify the electronic and power signals. It is also used as a switch for ON and OFF the electronic and power circuits (Myaing and Dinavahi, 2011). It is composed of a semiconductor material i.e. Ge, Si, Ga As and other semiconductor materials (Kejun Xia, *et al.*, 2012) Initially the circuit designers required a huge quantity of discrete transistors to implement them as discrete component to develop number of electronic circuits we can name such as amplifiers, differential amplifiers, power amplifiers, Inverters, dc choppers, Random access memory, Logic gates etc (Kularatna, 2006) Nowadays the millions of transistors and other components such as resistors, capacitors can also be fabricated on a single chip due to modern technologies of IC fabrication, in this way the cost and size of circuits as well as electronic equipment is reducing (Kwok, 2002)The idea of field effect can be traced back to Lilienfeld in 1926 (Lihenfeld, 1930-1933) and to Heil in 1935 (Heil, 1935). The first experimental FET was shown by Shockley and Pearson in 1948 (Shockley and Pearson, 1948).

2. MATERIALS AND METHODS

A GaAs FET device is fabricated using semi-insulating (S.I) substrate. In FET fabrication, a thin epitaxial layer of *n*-type GaAs is deposited on a semi-insulating GaAs substrate. The optimum value of doping concentration in the epi-layer depends on the maximum allowed gate leakage current. For a given doping concentration optimum value of active channel thickness, a is a function of gate length, L_G. It has been shown that optimum doping level for low noise *mm*-wave length device is ~ 5 x 10^{17} cm^{-3} (Itoh, et al, 1980). For a good gate length to channel thickness ratio (L_G / a) which is commonly known as the aspect ratio, should be in the range of 3-5 (Ladbrooke, 1991). For a low-noise FET smallest acceptable value of L_G / a is 3 (Brokerhoff and Heime ,1983). In *mm*-wave GaAs FETs where transconductance is of main importance and the devices are operated at comparatively low current and biasing

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voltage, gate recesses are usual. The cross-sectional view of GaAs FET is shown in **(Fig.1)**.

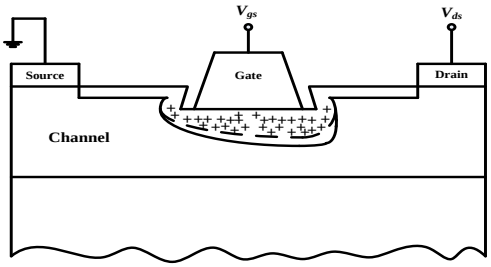

Fig.1. A cross-sectional view ofGaAs FET.

3. PROBLEM AND STATEMENT

GaAs field effect transistors (FETs) are widely used in high-technology analog and digital circuit devices due to their best noise and gain properties. There are many GaAs FET models used to predict their *I-V* characteristics (Golio M and Golio J, 1991). Usually, these microwave *I-V* models are divided based on the techniques employed in their development. These models are generally classified as:Numerical models and Physical models.The accuracy of numerical models is better of physical models but not suitable for applications in circuit design programs due to their complexity and more parameters. Design engineers prefers physical model because physical model can predict the device characteristics to a good accuracy (Rodriguez and England, 1992). The DC model of GaAs FET is generally accepted when it is based on device fabrication parameters for understanding the physical mechanism of operation in short channel microwave FET's.

There are many nonlinear GaAs FET models in the circuit design which are used in device simulation to predict the device dc characteristics (Curtice, 1980). All these microwave non-linear models are assuming an ideal Schottky barrier junction of the device, which have no interface states. A direct way to enhance the high frequency capabilities of a FET is the reduction of its gate-length, L_G (Rodriguez and England, 1992) which inevitably causes a finite density of interface states at Schottky barrier (Ahmed and Ladbrooke, 1995).

A shortcut way to increase the frequency capabilities of a FET device is the reduction of its L_G (Kacprzak and Materka, 1983) which predictably causes a finite density of interface states at Schottky barrier [22,23]. This work involves the study of five used nonlinear *I-V* GaAsFET models.The accuracy of these models is checked by simulating their DC characteristics for submicron GaAs FET's and comparison of their results with experimental data is also discussed. Models parameters are estimated by calculating root mean square (RMS) errors from experimental and simulated data. When a possible best fit for *I-V* characteristics is attained, then the values of $g_m$and$g_d$are simulated by using their respective expressions.

4. RESULTS AND DISCUSSION

The five different FET models are,Curtice (1980), Materka(1983), Statz (1987), Ahmed (1997) and Noor (2007). Their ability to simulate submicron GaAs FET's characteristics is checked by MATLAB. The accuracy of a model is reported by evaluating its RMS error values as a function of device biasing. The summary of these models is given in Table-1.

In 1980, Curtice proposed FET model (Curtice, 1980) for circuit simulation. This model is modified FET model for circuit simulator proposed by V. Tuyl in 1974 (Ahmed and Ladbrooke, 1995). The expression for *I-V* Characteristics of this model is given in Table-1 (Curtice, 1980). The comparative simulation results with experimental data are shown in **(Fig. 2)** shows the experimental (circled) and the predicted (solid line) *I-V* characteristics of a submicron GaAs FET by using Curtice model **(Fig.3)** shows that Curtice model performance is better in the linear region of operation. The Curtice model deteriorates significantly in the saturation region of operation. Therefore, for submicron GaAs FET's this model performance is not within minimum acceptable accuracy. Henceforth, one can conclude that Curtice model is not suitable to predict *I-V* characteristics of a submicron GaAs FET's.

V_T definition of Taki model (Taki, 1985) is modified by Materka for its V_{ds}dependence and he proposed a *I-V* characteristics model for GaAs FET given **(Table-1)** [18]. In eq.1 the hyperbolic tangent function goes to unity for higher values of V_{ds}which is the case when $V_{ds} \geq V_{sat}$, then expression for $\gamma = 0$ is reduced to Shockley Equation (Taki, 1987).

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_T}\right)^2 \qquad (1)$$

Hence, after the onset of current saturation Materka model expression is the same as that of Shockley square law expression. **(Fig.4)** represents *I-V* characteristics of a submicron GaAs FET by using Materka model. A poor match between the experimental (circled) and the predicted (solid line) characteristics demonstrate the failure of Materka model for simulation of devices. This is mainly due to the inability of the model to simulate finite value of $g_d$in the saturation region of operation, which is generally observed

Table-1.*I-V* Model Expressions for Different DC Models of GaAs FET

S. No.	Model Name	*I-V* Characteristics Expression
1	Curtice Model (1980)	$I_{ds} = \beta (V_{gs} - V_T)^2 \times \tanh(\alpha V_{ds})(1+\lambda V_{ds})$
2	Materka Model (1983)	$I_{ds} = I_{dss}\left[1 - \frac{V_{gs}}{V_T + \gamma V_{ds}}\right]^2 \times \tanh\left(\frac{\alpha V_{ds}}{V_{gs} - V_T - \gamma V_{ds}}\right)$
3	Statz Model (1987)	$I_{ds} = (1+\lambda V_{ds})\left[\frac{\beta (V_{gs} - V_T)^2}{1+\delta (V_{gs} - V_T)}\right] \times \left[1 - \left(1 - \frac{\alpha V_{ds}}{3}\right)^3\right]$ *for* $0 < V_{ds} < \frac{3}{\alpha}$ $I_{ds} = (1+\lambda V_{ds})\left[\frac{\beta (V_{gs} - V_T)^2}{1+\delta (V_{gs} - V_T)}\right]$ *for* $V_{ds} \geq \frac{3}{\alpha}$
4	Ahmed Model (1997)	$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right)^2 \times \tanh(\alpha V_{ds})(1+\lambda V_{ds})$
5	Noor Model (2007)	$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{(1+\eta e^{V_{gs}})(V_T + \Delta V_T + \gamma V_{ds})}\right)^2 \times \tanh(\alpha V_{ds})(1+\lambda V_{ds})$

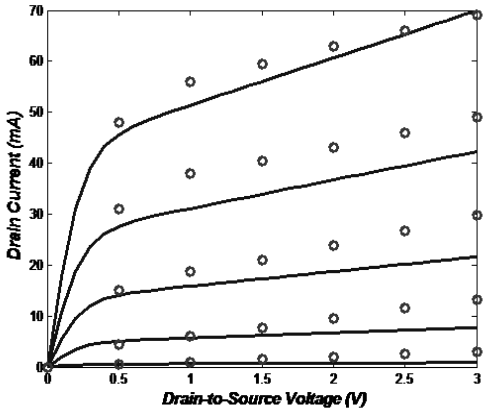

Fig. 2.Experimental and predicted I-V characteristics ofGaAs FET by using Curtice nonlinear dc model.

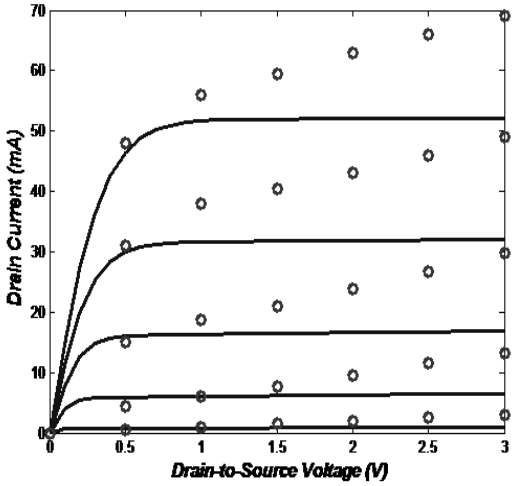

Fig. 3.Experimental and predicted I-V characteristics of GaAs FET by using Materka nonlinear dc model.

in short- channel submicron FET's. Statz proposed a FET model (Newman, *et al.,* 1987) to simulate *I-V* characteristics by using the expression given in Table1.The Statzmodel simulation of output characteristics of a FET is fairly complicated in comparison with two models i.e., Curtice and Materka Model. It is polynomial in nature and difficult to manage. The basic parameters of a physical model have been treated in a complicated way and the rule of square given by the Shockley's equation has been violated.**(Fig. 5)** represents the predicted (solid line) and the experimental (circled) characteristics for a submicron GaAs FETs. A poor match between the observed and the simulated characteristics demonstrates the inability of Statz model to predict the response of a submicron GaAs FET. Review of the **(Fig.5)** shows that Statz model exhibit poor gate control that could be one of the main causes which have led to a significant discrepancy as is seen in previous two plots. Ahmed proposed a model (Ahmed and Ladbrooke, 1997) to simulate *I-V* characteristics for short channel GaAs FET, The expression for *I-V* Characteristics of this model is given in Table 1((Ahmed, *et al.,* 1997). According to simple one-dimensional device models, the value of V_T is independent of L_G (Ladbrooke, 1995). But in fact V_T is a function of L_G in short channel devices (Rodriguez and England, 1992). The main contribution of Ahmed model is that it has introduced a change in V_T caused by the geometry of the

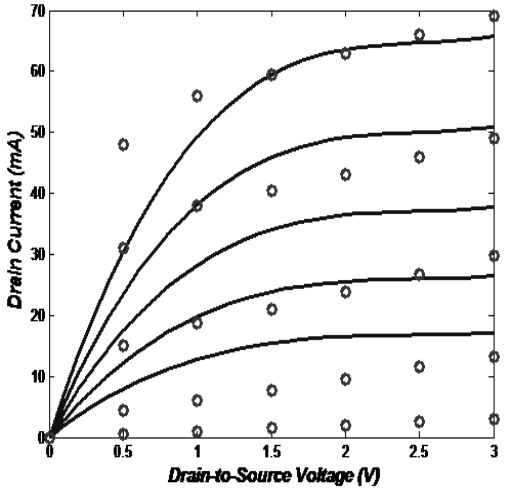

Fig.4.Experimental and predicted I-V characteristics of GaAs FET by using Statz nonlinear dc model.

submicron device into expression of the model with a term ΔV_T defined by:

$$\Delta V_T = \frac{4a}{3L_g} V_T \qquad (2)$$

(Fig. 6) shows the experimental (circled) and predicted (solid line)*I-V* characteristics for a submicron GaAs FET by using Ahmed model. Comparing it with the models previously reported, it is clear that the performance of Ahmed model is significantly better. This Model is an extension of Ahmed Model (Ahmed, *et al.,* 1997). It is used to simulate *I-V* characteristics for short channel GaAs FETs. This model was proposed by Memon in 2007. The expression for *I-V* Characteristics of this model is given in Table 1 (Memon, 2007). **(Fig. 6)** shows the experimental (circled) and predicted (solid line) *I-V* characteristics for a submicron GaAs FET by using Noor model. Comparing it with the models previously reported, it is clear that the performance of Noor model is significantly better of the other models.

RMS error values were calculated at different V_{qs} voltage for the *I-V* models under consideration, as indicated in Table 1 are given in Table 2.It has been observed that Noor model offers lowest RMS errors i.e., 0.60, whereas the worst observed case is the Statz model has average RMS errors as a function V_{qs} 5.03. Ahmed model offered RMS error close to Noor model i.e., 0.66. This shows that one of these two *I-V* models could be a suitable choice for circuit designers with submicron GaAs FETs. However, amongst those Noor model performance is the best observed one for short channel GaAs FETs.

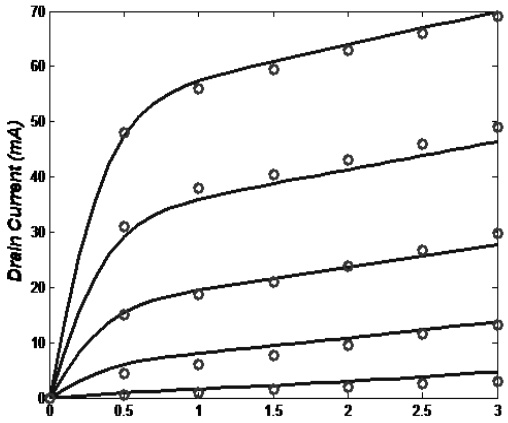

Fig.5. Experimental and predicted I-V characteristics of GaAs FET by using Ahmed nonlinear dc model.

Furthermore, Noor model has one more of fitting variable compared with Ahmed model due to which fitting, Noor Model with experimental one is better than Ahmed model. Thus, it should be a preferred model for circuit designers with submicron GaAs FETs.

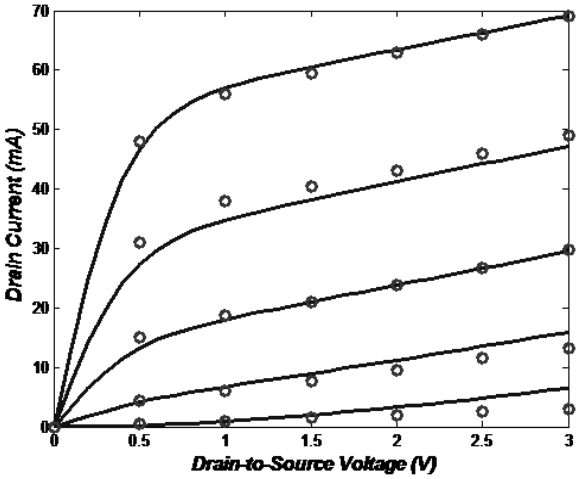

Fig. 6: Experimental and predicted I-V characteristics of GaAs FET by using Noor nonlinear dc model.

5. CONCLUSION

In this paper we discussed the comparison of submicron GaAs FET's DC Models and their AC analysis. Five different FET models were presented and their ability to simulate submicron GaAs FET's characteristics was checked in MATLAB.These models were examined and discussed by considering the variables involved in their definition along with fitting parameters.

To demonstrate the validity of a model, I-V characteristics of short channel FETs, the simulated results were compared with experimental data. The accuracy of a model is reported by evaluating its RMS

error values as a function of device biasing. It is noted that the Noor model, when applied to high frequency FETs, offers better simulation results compared to other models under consideration. Whereas, the simulated results of Ahmed model are close to the Noor model. **(Table 2)** Therefore these two models may be used to simulate the *I-V* Characteristics of submicron GaAs FET's.

Table 2. Comparison Of Rms Errors Of Different Gaas Fet Models As A Function Of V_{gs}.

S. No.	Model	RMS error at different V_{gs}values					Average Error
		-0.8	-0.6	-0.4	-0.2	0 V	
1	Curtice	1.26	2.45	3.77	4.15	1.29	2.58
2	Materka	1.25	2.75	4.22	6.15	6. 20	2.87
3	Statz	6.95	6.89	5.38	3.18	2.74	5.03
4	Ahmed	0.56	0.45	0.52	0.93	0.85	0.66
5	Noor	0.62	0.48	0.21	0.87	0.85	0.60

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