Sindh Univ. Res. Jour. (Sci. Ser.) Vol.45 (4) 743-748 (2013)

SINDH UNIVERSITY RESEARCH JOURNAL (SCIENCE SERIES)

Non-Linear model of the Second Order Voltage And Current Switched CP-PLLs

E. ALI, G. MUSTAFA*, K. B. AMUR, N. NIZAMANI, A. R. KHATRI, T. R. MEMON

Quaid-e-Awam University of Engineering, Science & Technology Nawabshah, Pakistan

Abstract: The charge-pump phase locked loop (CP-PLL) circuit is most suitable technique used to align the two signals in different applications in communication. The CP-PLL is mostly feasible because of its low cost, integerable and precise features. The charge-pump produces an error current, which is then integrated by the following loop filter. The error current is constant if the charge-pump is based on constant current sources however the pump current varies in the case of voltage switched charge-pump (VSCP). The conventional gain of detecting unit is directly proportional to the error current. It behaves non-constantly when the voltage switched charge pump (VSCP) structure is used. Hence, the pump current applied to the loop filter (LF) is no more constant. This latent peculiarity in the form of non-constant pump current delivered from the VSCP influences the system dynamic. In this paper, it is focused on comparing the transient dynamics of the second order CP-PLL system considering the current output of the both charge-pump circuits. The simulation results are achieved using discrete time non-linear event driven model considering the balanced and unbalanced pump current situations.

Keywords*:* Phase- locked loop, Non-linear discrete time model, voltage switched charge pump.

1. INTRODUCTION

The charge-pump phase locked Loop (CP-PLL) is a common component of modern electronic systems for different applications like frequency generation, synchronization, jitter suppression, clock and data recovery circuits Gardner (1980), Best (1984) Margaris (1985), Brain (1996). The PLL is a feedback system used to align two signal sources. One signal source is external (i.e. reference oscillator and other is the local oscillator inside the loop). The phase detector detects the phase difference two incoming signal at it inputs. The charge-pump with current switch (CSCP) produces ideally a balance pump current $i_p(t)$ while speeding up and slowing down the loop and it allows a suitable dynamics.

The most commercial PLL chips (like 4046) integrate a voltage switched charge pump (VSCP), because design using voltage source is simple and low manufacturing cost. Using a VSCP adds a curious non-linear effect arising in form of variations in the pump current as function of the electrical load of loop filter Gardner (1980), Best (1984), Margaris (1985) and Ehsan (2012). To analyse these effects during non-linear acquisition and locking process, it requires a systematic approach. Mixed analog and digital nature of the CP-PLL makes it more difficult to study the non-linear transient of the CP-PLL using any classical theory Hedayat, *et al* (1999), Brain, *et al* (1996). So different modeling techniques to simulate and analyse the behavior of the CP-PLL exist, e.g. linear models (continuous time and discrete time) described by Gardner (1984) and descand discrete time non-linear models described by Paemal (1994), Hedayat (1997), Hedayat (1999), Wiegand (2011), Ehsan (2012), and Ehsan (2013). Most of the time, linear models are engaged in verifying the designs, by approximating the non-linear characteristics of the PFD in a quasi-continuous time, but linear approach is valid only for very small phase variations in the locked state. The discrete-time non-linear models are more efficient and simplified, and powerful for the verifying designs, characterization and analysis Acco (1999), Daniels (2004), Hangmann (2013). In this paper, the discrete time non-linear second order voltage switched loop of the CP-PLL is compared with its equivalent current switched system using the non-linear Event Driven (ED) model to see how the pump current behaves using voltage structure of the system and its implications at different operating points are considered.

2. MATERIALS AND METHODS

The general architecture of the second order CP-PLL is represented in **Fig.1** and further detail of each system level components is given below:

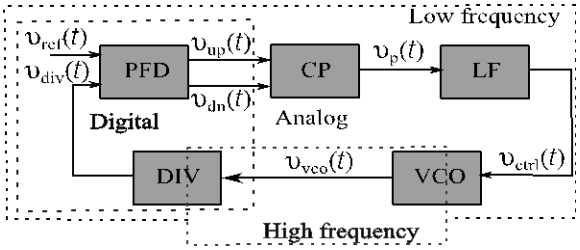


Fig.1: The basic architecture of the CP-PLL.

*Aalborg University, Denmark

2.1 Phase and Frequency Detector (PFD): The phase and frequency detector is frequently used phase comparator with improved characteristic over the other (X-OR and JK) phase detectors having two digital outputs ($\upsilon_{up}(t)$ and $\upsilon_{dn}(t)$) pulse whose duration is proportional to the sampled phase error, referrer to Best (1984), Brain (1996). Several sequential implementation of the digital phase detector exists, we will consider the intuitive architecture (**Fig.2**), which is based on two D flip-flops (with an additional and gate) triggered by the falling edges of the reference signal $\upsilon_{ref}(t)$ and the feedback signal $\upsilon_{div}(t)$ (in this paper only falling edges are considered). The D-flip-flop associated to the reference signal has an output called UP and the D-flip-flop associated to the feedback signal has an output called DOWN (in short DN). By considering these two binary outputs of the D-flip-flops, a finite state machine with three states is constituted Hedayat, (1997), Hedayat, (1999).

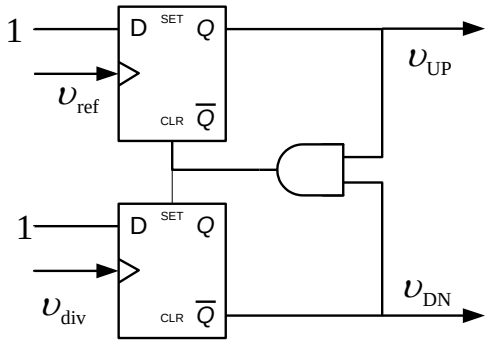


Fig 2: The digital phase and frequency detector circuit.

2.2. Charge-Pump (CP): The CP encodes the phase error error detected by PFD into an analog signal (current or voltage), which then excites the LF as given in Gardner, (1980), Best, (1984), Margaris, (1985), Hedayat, (1997), Ehsan, (2012). Fig. 3 represents two configurations different charge pump circuit. The VSCP shown in Fig.3(a) is realized by two constant voltage sources and it produces a varying current ($i_p^{vs}(t)$) as a

$$i_p^{vs}(t)=\begin{cases}\dfrac{V_{DD}-\upsilon_{C1}(t)}{R_0+R_1} & \text{if } S_{+1}\\ 0 & \text{if } S_0\\ \dfrac{V_{SS}-\upsilon_{C1}(t)}{R_0+R_1} & \text{if } S_{-1}\end{cases}\quad i_p^{cs}(t)=\begin{cases}+I_P & \text{if } S_{+1}\\ 0 & \text{if } S_0\\ -I_P & \text{if } S_{-1}\end{cases}\qquad (1)$$

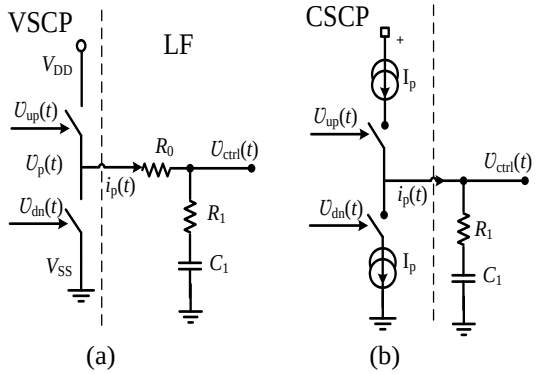


Fig 3. (a) The voltage switched charge-pump with lead-lag filter (b) The current switched charge-pump with simple RC filter.

Function of the electrical load of the LF. The current switched CP (CSCP) produces an ideal constant current, however the design of the constant current source is very involving. In most commercial PLL ICs, designers prefer the VSCP topology due to its low cost and easier design. The pump current produces by both CPs topologies is represented in (1).

2.3. Loop Filter (LF): The low pass filter is used to smooth signal coming from the PFD-CP unit and suppresses the higher order harmonics in the PFD-CP output signal and passes the low order harmonics only as defined by Gardner (1980), Margaris, (1985), Ehsan, (2012), Hedayat, (1997). The LF shown in **Fig.3(a)** is a dimension less filter used in VSCP topology (Best, 1984). The LF shown is **Fig.3(b)** is used with current switched structure of the PLL. Both LFs are represented by linear, non-autonomous and time invariant differential equations. To solve the general solution of the $\upsilon_{ctl}(t)$,

$$\Sigma\text{LF}:\begin{cases}\dot{x}(t) = \text{A}\,x(t)+\text{B}\,u_p(t)\\ \upsilon_{ctl}(t)=\text{C}^T x(t)+\text{D}\,u_p(t)\end{cases}\qquad (2)$$

where the matrices A, B, C and D are defined for each LF as

$$\text{A}^{vs}=-\frac{1}{(R_0+R_1)C_1}\qquad \text{A}^{cs}=-\frac{1}{R_1C_1}$$

$$B^{vs}=\frac{1}{(R_0+R_1)C_1}\qquad B^{cs}=\frac{1}{R_1C_1}$$

$$C^{vs}=1-\frac{R_1}{(R_0+R_1)}\qquad C^{cs}=1$$

$$D^{vs}=\frac{R_1}{(R_0+R_1)}\qquad D^{cs}=R_1$$

and $u_p(t)$ is $i_p(t)$ in case of CSCP and $\upsilon_p(t)$ in case of the VSCP configuration.

2.4. Voltage Controlled Oscillator (VCO): The VCO produces an output signal having a frequency proportional to the voltage applied to its input (Paemal, 1994; Hedayat, *et al*, 1997;). Ideally, the transfer characteristic of the VCO is a linear function of the input voltage υ_{ctrl}.

$$\omega_{vco}(\upsilon_{ctl}(t)) = K_{v,\omega}\upsilon_{ctl}(t) + \omega_{v\phi} \quad (3)$$

Where ω_{vco} the angular frequency of the VCO is, $K_{v,\omega}$ is the gain (in rad/sec/V) and $\omega_{v\phi}$ is the free running angular frequency (**Fig.4**).

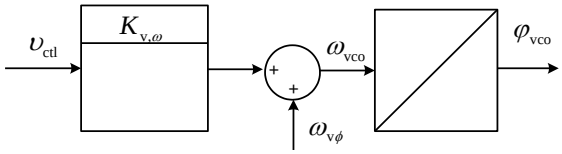


Fig 4: The representation of the linear phase of the VCO

$$\phi_{vco} = \int_{t_j}^{t_{j+1}} \omega_{vco}\left(\upsilon_{ctl}(t)\right) dt \quad (4)$$

2.5. Frequency Divider (DIV): The PLL is vastly used in many applications to perform frequency synthesis, then a frequency divider is implemented in the loop as explained in references Hedayat (1997), Paemal (1994), and Brain, (1996). If its division ratio is given by an integer N **(Fig.5,6),** then the following frequency is generated from the VCO in the steady state:

$$\omega_{ref} = \omega_{div} \Rightarrow \frac{1}{N} \bullet \omega_{vco} \quad (5)$$

The principle of the ED technique is mostly based on calculating the phase of an event falling from the reference and divider signal. This forcing event is actually triggering the PFD to compensate the phase error to lock and settle the PLL to a desired frequency, the technique is well explained in Hedayat (1997), Hedayat (1999), Wiegand (2011), Ehsan (2012), and Ehsan (2013).. The event driven model is actually calculating the phase of the reference (ω_{ref}) and divider signals (ω_{div})

$$\phi_{ref}\left(t_{j+1}\right) = \phi_{ref}\left(t_j\right) + \int_{t_j}^{t_{j+1}^{ref}} \omega_{ref}\left(t'\right) dt' \quad (6)$$

$$\phi_{div} = \phi_{div}\left(t_j\right) + \int_{t_j}^{t_{j+1}^{div}} \omega_{div}\upsilon_{ctrl}\left(t'\right) dt' \quad (7)$$

respectively when a falling event complete cycle:

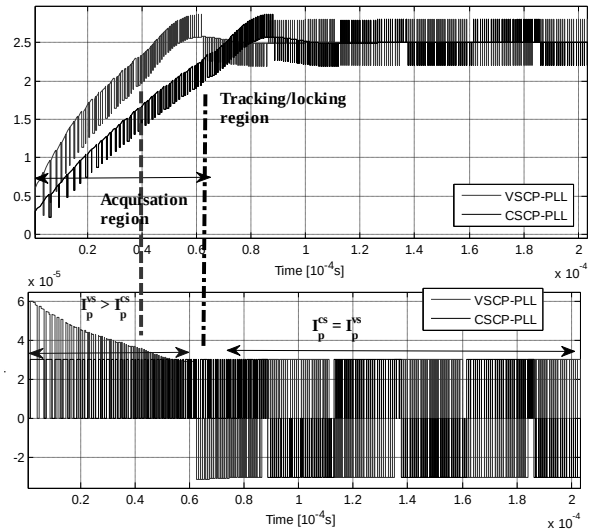


Fig. 5. The transient behavior of both system converging to a target value is $\upsilon_{ctl} = V_{DD}/2$.

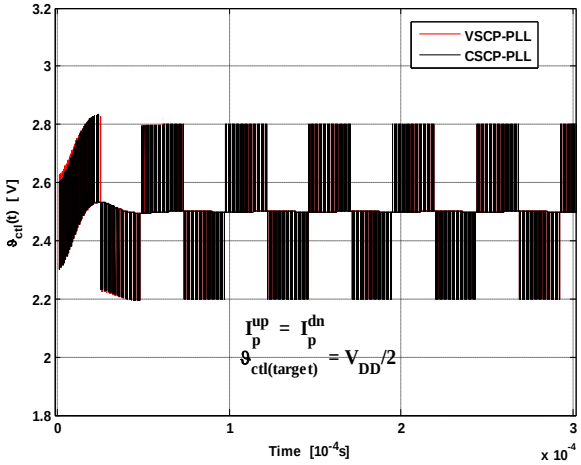


Fig. 6: With initial conditions close to the target value, both system are nearly similar in dynamics at $\upsilon_{ctl(target)} = V_{DD}/2$.

$$\phi_{ref}(t_{j+1}^{ref}) \overset{!}{=} 2\pi \quad (8)$$

$$\phi_{div}(t_{j+1}^{div}) \overset{!}{=} 2\pi \quad (9)$$

t_{j+1}^{ref} represents instant of a falling event the reference oscillator. t_{j+1}^{div} represents instant of a falling edge of the divider signal.

The effective falling edge is the calculated using minimum operator:

$$t_{j+1} = \min(t_{j+1}^{div}, t_{j+1}^{ref}) \quad (10)$$

For a constant or varying (i.e. ramp) reference frequency, (8) leads to a simple analytical solution for an event falling at t_{j+1}^{ref}. When considering the current switched charge-pump, the divider phase equation is quadratic and the expression (9) also leads to an

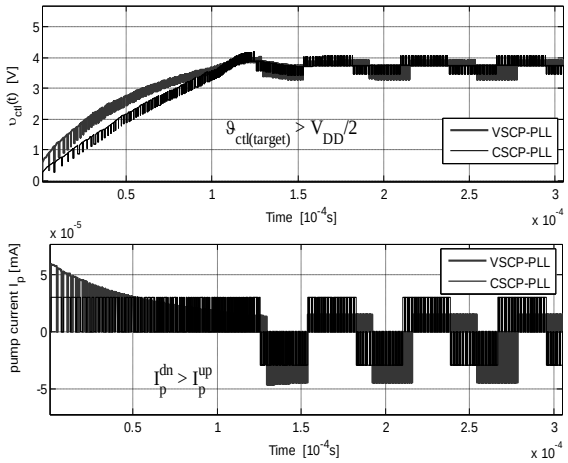


Fig. 7. The locked dynamics of both system near to target value at $\upsilon_{ctl(target)} > V_{DD}/2$.

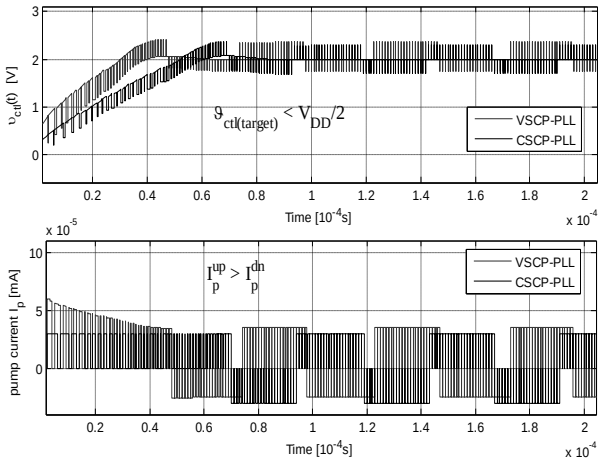


Fig. 8. The locked dynamics of both system near to target value at $\upsilon_{ctl(target)} < V_{DD}/2$.

analytical solution for t_{j+1}^{div}. However for the voltage switched CP-PLL (VSCP-PLL), the equivalent feedback divider phase equation is non-analytic and needs to calculate t_{j+1}^{div} numerically.

3. RESULTS AND DISCUSSION

The dynamic behavior of the both systems is explored using the ED simulations. In this paper the simulated transient behavior of both system level CP-PLLs is compared in two situations (a) where the pump current behaves symmetrical in the settled state and (b) when it behaves as asymmetrical in the settled state.

3.1. Balanced pump currents in steady state

The voltage switched structure of the charge-pump delivers a non-constant pump current (1) due the electrical load of the LF. As soon as the potential at control node (at the input of the VCO) increases, the pump current becomes small. The charge-pump current is equal in the state up and down at $\upsilon_{ctl(target)} = V_{DD}/2$ where PLL is settled. Fig.5 shows the control voltage settling behavior of the loop and it is very clear that, for the VSCP-PLL architecture initially the pump current is high, as soon as input of the VCO reaches the target voltage the current becomes equal in the up half-cycle and the down half-cycle. In the beginning, the voltage system is faster in dynamics because higher pump current is supplied. In the steady state, both systems have almost similar current as $i_p^{up} = i_p^{dn}$ (**Fig. 5** second part). By keeping initial conditions near to locking, both systems are nearly equal in current and the symmetric transient behavior of both systems is shown in **(Fig.6)**.

3.2. Unbalanced pump currents in steady state

When the CP-PLL is locked and settled above or below the average value of the CP supply range, it exhibits asymmetrical dynamics. The pump current in the up and down half-cycles behaves unbalanced. As an example, the transient behavior is simulated for the situation where the system locks at $\upsilon_{ctl(target)} > V_{DD}/2$. It can be seen that (**Fig. 7**), the pump current in the down half-cycle is higher than the up half-cycle. The VSCP-PLL dynamics is bit slowly converging to the target value than the current switched system. In one more situation, when the system locks at the target value $\upsilon_{ctl(target)} < V_{DD}/2$, consequently the pump current in the up half-cycle is higher than the down half-cycle (**Fig. 8**). It is obvious that, the up half-cycle dynamic is more rapid than the down half-cycle. The locking and settling time of the VSCP-PLL is less than the CSCP-PLL, since it contains more current initially (see Fig.5 and Fig.8), however it can be seen in Fig.7, both system settles at nearly same time. As soon as $\upsilon_{ctl(target)} > V_{DD}/2$, the pump current is growing week so the PLL operating with current pump is settling before the VSCP-PLL. It is evident that the dynamical response of the voltage switched system holds peculiarity in the form of unbalanced pump current, which can be critical in locking and frequency tracking applications. Therefore, designers have to take in account an inherent pump current constraint with voltage switched structure, which may result as a serious constraint in several applications which requires robust dynamic of the CP-PLL system. The effect of different current situation on the stability using GARDNER's approach for voltage switched charge-pump was shown in Ehsan, (2013).

4. CONCLUSION

A comparison concerning the pump current output in two different topologies of CP-PLL was presented. The curious nonlinearity that arises from the part of voltage switched charge-pump results in an unbalanced current pumping to the loop filter. This peculiarity could be very serious in applications like

frequency tracking where robustness in dynamic of the system is demanded from the design point of view. The current switched CP-PLL has obviously a constant dynamics at any target value of the control voltage. But the design of the current source is more difficult and involving than a voltage source. The designer must be careful to take into account the pump current requirements to meet a desired accuracy for frequency tracking applications.

REFERENCES:

Ali E., W. Rahajandraibe, F. Haddad, C. Hangmann, and C. Hedayat (2013). Simulative stability characterization of the Second Order Voltage Switched CP-PLL, IEEE MWSCAS, OH, USA, 153-156.

Ali E., C. Wiegand, C. Hangmann, C. Hedayat and D. Kraus (2012). Event Driven Simulation of the Second Order Voltage Operated CP-PLL, SAME conference, 2-3, Nice France.

Acco P., M. P. Kennedy, C. Mira, B. Morley, Frigyik (1999). Behavioral modeling of charge pump phase locked loop, ISCAS Jul 1999, **01**, 375 - 378.

Brain A. F. Antao, M. Turky and R. H. Leonowich (1996). Behavioral Modeling Phased Locked Loop for Mixed-Mode Simulation, Analog Integrated Circuits and Signal Processing, @ Kluwer Academic Publishers Boston. Manufactured in The Netherlands

Best R. E. (1984). Phase Locked Loop Design, Simulation and Applications, McGra Hill New York 2nd Edition.

Daniels B. R., G. Farrell, Baldwin (2004). Arbitray order Charge approximation event driven phase-lock loop model, ISSC 2004, Belfast, June 30-July 124-128.

Gardner, F. M. (1980). Charge Pump Phase Locked Loop, IEEE Transaction Communications, vol 28(11), 1849-1858.

Hangmann, C., C. Hedayat, and U. Hilleringmann (2013). Enhanced event-driven modeling of a CP-PLL with nonlinearities and nonidealities, IEEE MWSCAS, OH, USA, 309 - 312

Hedayat C., H., Ahmed, Y Leduc and G., Benbassabt (1997). High Level Modeling applied to second order charge-pump PLL circuit, TI Technical Journal, 100-108.

Hedayat C., H. Ahmed, Y Leduc and G. Benbassabt (1999). Modeling & Characterization of the 3rd Order Charge-Pump PLL: a Fully Event-driven Approach, Analog Integrated Circuits and Signal processing 19, 25-45.

Margaris I.N. and V. Petridis (1985). Voltage Pump Phase-Locked Loops, IEEE Transactions on Industrial Electronics, 32 (1), 41-49.

Paemal M. V. (1994). Analysis of a Charge-Pump PLL: New Model, IEEE Trans. on Comm., 42, 2490-2498.

Wiegand C., C. Hangmann, C. Hedayat, and U. Hilleringmann (2011). Modeling and Simulation of Arbitrary Ordered Nonlinear Charge-Pump Phase-Locked Loops, Semi-conductor Conference Dresden.