Sindh. Univ. Res. Jour. (Sci. Sr) Vol: 30 (1) 19-23 (1998)

SIMULATION STUDY AND MODEL OF FAULT-DETECTION IN COMBINATIONAL CIRCUITS

M. Nawaz Brohi and Imran Ujjan

Institute of Mathematics and Computer Science, University of Sindh, Jamshoro.

ABSTRACT

This paper is concerned with the simulated study of faulty combinational circuits and presenting its rectified simulated model in case of detection of any fault by using preset fault-location experiment in C-Language.

Key Words: Nonideal trainsient behaviour; stuck-at-one, stuck-at-zero.

Introduction to combinational Circuit

A combinational circuit consists of logic gates whose outputs can at any time be determined directly from the present combination of inputs without regard previous inputs. A combinational circuit performs a specified logically by set of Boolean functions[1].

Types of Faults

Digital system suffers two classes of faults: temporary faults, which occur due to noise and the non ideal transient behaviour of switching components, and permanent faults, which result from component failures.

The Fault

One way of determining whether a combinational circuit operates properly is by applying to the circuit all possible input combinations and comparing the resultant outputs with either the corresponding truth table or a faultless version of the same circuit. Any deviation indicates the presence of some faults. Moreover, if a known relationship exists between the various possible faults and the deviations of output patterns, it is possible to diagnose the fault and to classify it at least within a subset of faults whose effects on the circuit output are identical.

In the circuit most commonly used at present an open connection is logically equivalent to have that connection either "stuck-at-one" or "stuck-at-zero". In designing fault detection tests we shall be concerned only with those faults which cause any wire to be stuck-at-zero or stuck-at-one (abbreviated s-a 0 and s-a-1).

Restricting our consideration to just this class of faults is technically justified, since most circuits failures fall in this class, and many other failures exhibit symptomatically identical effects.

Simulated Study

The Fault Table

Let $X_1, X_2, \ldots, X_n$ be the inputs to a combinational circuits and let f be its fault-free output. Let $f\alpha$ denote the output of the circuit in the presence of fault α. Consider the circuit shown in fig.1 (a) and suppose that any one of its wire m, n, p and q may be either s-a-1. We shall denote by m_0 and m_1 the faults of wire m s-a-0 and s-a-1, respectively. Similar notation is used is used for the other wires. The truth table for this circuits is shown in fig.1 (b), where column f denotes the fault α free output while, columns fm_0 and fm_1 correspond, respectively, to the circuit in the presence of faults m0 and m1, and so on.

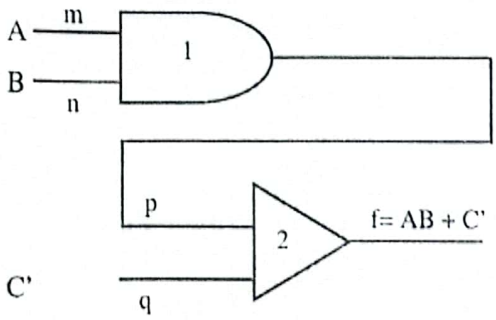


Fig. 1 (a) Circuit to be tested

* Department of Statistics, University of Sindh, Jamshoro.

Inputs ABC	F	Outputs in presence of faults							
		fm_0	fn_0	fp_0	fq_1	fm_1	fn_1	fp_1	fq_1
000	1	1	1	1	0	1	1	1	1
001	0	0	0	0	0	0	0	1	1
010	1	1	1	1	0	1	1	1	1
011	0	0	0	0	0	1	0	1	1
100	1	1	1	1	0	1	1	1	1
101	0	0	0	0	0	0	1	1	1
110	1	1	1	1	1	1	1	1	1
111	1	0	0	0	1	1	1	1	1

Fig.1 (b) Truth table for the fault-free output and outputs in the presence of faults.

An input combination is referred to as a test for fault fα if, in response to that input combination, the output of the correctly operating circuit is different from that of the circuit impaired by fault fα. Hence the input combination 111 is the only test for detecting the fault fmo in the circuit of fig.1 (a), since it is only input combination for which the values in columns f and fm_0 are different. On the other hand, fault fq1 can be detected by the test 001, 011, 101 and so on, for other faults. More precisely, an input combination a_1, a_2, …, an is a test for detecting fault f α if and only if.

$$F(a_1, a_2, \ldots, a_n) \oplus f\alpha(a_1, a_2, \ldots, a_n)=1$$

Where f (a_1, a_2, …, a_n) and fα (a_1, a_2, …, a_n) denote respectively, the fault free output and output in response to the input a1, a2, … an. Thus, in order to determine all the tests that detect a fault fα, it is necessary to take the modulo-2 sum of columns f and fα in the truth table.

If we combine equivalent faults table and take the modulo-2 sum of column f with all other column which correspond to incorrect outputs, we obtain the fault table shown in fig.1 (c).

This table is valuable tool in determining the minimal set of tests for detecting all the faults in the circuit of fig.1 (a).

Results and Discussion

Fault-Location Experiments

To locate, or diagnose, a fault it is not only necessary to detect it, but the fault must also be distinguish from all other nonequivalent faults. This can be accomplished by means of an expanded fault table which will subsequently be refereed to as the fault-location table. We shall consider two types of experiments:

1. Preset experiments, in which the entire set f tests is predetermined independently of the circuit's response.
2. Adaptive experiments, in which the test to be presently applied depends on the response of the circuit to proceeding test.

Present Experiment

The fault-location table consists of all the rows and columns of the table (detection) table and in addition, it consists of a new column for each pair of faults of the fault table. Thus, if a fault table has K columns, the corresponding fault-location table will have K+K (K-1)/2 = K(K+1)/2 columns f_i and f_j.

Consider the fault table shown in Fig.2(a). It consists of six rows T_1, T_2, …, T6 corresponding to six possible tests, and six columns f_1, f_0, …, f_6 corresponding to six faults. By taking fault all pair wise modulo-2 sum of these columns we obtain entire fault-location table of Fig.2(a). the –entires of column f_if_j, indicate the tests that distinguish between faults f_1 and f_j, since either f_i and f_j (but not both) can be detected by each of these tests.

	f1 f2	f1 f3	f1 f4	f1 f5	F1 f6	f2 f3	f2 f4	f2 f5	f2 f6	f3 f4	F3 F5	f3 f6	f4 f5	f4 f6	f5 f6
T1				1	1			1	1		1	1	1	1	
T2	1		1		1	1		1		1		1	1		1
T3			1	1			1	1		1	1			1	1
T4	1	1					1	1	1	1	1	1			
T5	1	1	1	1					1					1	1
T6	1		1	1		1			1	1				1	1

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	F1	f2	f3	f4	f5	f6	f1 f2	f1 f3	f1 f4	f1 f5	f1 f6	f2 f3	f2 f4	f2 f5	f2 f6	f3 f4	f3 f5	f3 f6	f4 f5	F4 f6	f5 F6
T1					1	1				1	1			1	1		1	1	1	1	
T2	1		1		1		1		1		1	1		1		1		1	1		
T3				1	1				1	1			1	1		1	1		1	1	
T4		1	1				1	1					1	1	1	1	1	1			
T5	1					1	1	1	1	1					1			1		1	1
T6	1		1			1	1		1	1		1			1	1	1			1	1

Fault Table

Fig.2(a) Fault-Location Table.

To find a minimal set of fault-location tests that covers this table, we first identify T_3 and T_4 as the essential tests. The elimination of the essential rows and the (check-marked) columns covered by them yields the reduced table of Fig.2(b). Columns f_4f_5 can be eliminated since it becomes equivalent to column f_1f_6. Row T_5 can be eliminated because it is dominated by row T_6, and subsequently, column f_2f_3 can be eliminated since it becomes equivalent to column f_1. The final table can be covered by any two of three tests T_1, T_2 and T6. If we choose T_2 and T6 and add them to the essential tests, we obtained the complete set of preset fault-location tests {T_2, T_3, T_4, T_6}.

	f_1	F_2	f_3	f_4	f_5	f_6
T1					1	1
T2	1		1			1
T3				1	1	
T4		1	1			
T5						1
T6			1			1

In the case of preset fault-location experiments, it is convenient to have a fault dictionary which consists of a listing of the circuit outputs when any of the possible faults occur. The fault dictionary for the outputs of the fault-free circuits shown in Fig.3(a) is given in Fig.2(c).

Inputs	Outputs in presence of faults				
ABC	{m_0, n_0, p_0}	q_0	M_1	n_1	{p_1,q_1}
000		1			
001					1
010		1			
011			1		1
100		1			
101				1	1
110					
111	1				

Fig 1. (C) Fault Table

Fig. 1. Derivation of minimal set of fault-detection tests.

Input the # of tests (1-6):6

Input the # of faults (1-6):6

You are required to give the particular (6) faults for each TEST.

Press 1 when a fault exits and ENTER otherwise Press any key.

Press any key to have a look at all faults due to 6 faults per test.

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Test T4 is essential because fault 2 is only being covered by this TEST.

Test T3 is essential because fault 4 is only being covered by this TEST.

	f1	f2	f3	f4	f5	f6	f7	f8	f9	f 10	f11	f12	f13	f14	f15	f16	f17	f18	f19	f20	f21
T1											1								1		
T2	1										1	1							1		
T3																					
T4																					
T5	1					1															
T6	1		1			1						1									

	Faults				
Test	f1	f6	f1f6	f2f3	f4f5
T1		1	1		1
T2	1		1	1	1
T5	1	1			
T6	1	1		1	

Fig.2(b) Simulated table

Fault	Test			
	T2	T3	T4	T6
f	1	0	1	1
f1	0	0	1	0
f2	1	0	0	1
f3	0	0	0	0
f4	1	1	1	1
f5	0	1	1	1
f6	1	0	1	0

Fig.2.(c) Fault dictionary for preset experiment
For the circuit output shown in Fig.3(a).
Fig.2 Derivation of a minimal preset fault-location experiment.

Test	Faults							Output
	f0	f1	f2	f3	f4	f5	f6	Of Fault free Circuit
T1						1	1	0
T2		1		1		1		1
T3					1	1		0
T4			1	1				1
T5		1					1	0
T6		1		1			1	1

Fig.3(a) Fault Table.

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Simulation Model

We have built a simulated model for faulty combination circuit by using preset fault-location experiment in the C-Language.

Conclusion

In most practical situation the circuit is constructed of modules and it is only required to locate the faults within the limits of the modules. In such cases if a fault is located within a certain module, the entire module is replaced and hence it is not necessary to distinguish among faults which occur within the same module. Suppose that faults f_1 and f_6 of Fig.2(b) occur within the same module and faults f_4 and f_5 occur within another module. Consequently, both columns f_1f_6 covered by test T_6. In this case the entire fault-location experiment consists of three tests $\{T_3, T_4, T_6\}$.

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