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Control of voltage stress, conduction loss and switching losses through comparison between Hardware design and Simulation of 9 level and 13 level Inverter in APOD strategy

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Abstract: Power electronics devices such as inverters has been get too much importance because of their numerous advantages like change in voltage, harmonic distortion, switching loss and efficiency. When converting DC to AC, we want to achieve required voltage and frequency. While converting DC to AC we generate our required output voltages and frequency but it causes harmonic distortion. This harmonic distortion can be reduced by introducing multilevel output, which reduces change in voltage, and increase efficiency by staircase voltage levels. Two level inverter can produce only 0 level and any other voltage level but two level inverter is not suitable for higher frequency and higher voltage applications. Output voltage of inverter should be pure sinusoidal waveform without harmonics but practically sine wave has harmonics. In hardware design parallel DC source, bidirectional switches, and large capacitance values are used in order to increase performance efficiency and reduces harmonics. In this paper Nine level and thirteen level inverter efficiency is improved on hardware by applying optocoupler and capacitor techniques with higher input voltage and higher load applications, then hardware results are compared with simulation results. Capacitors are used before optocouplers which isolates input from output and gets signal from Arduino which is applied at MOSFETS. Control circuit requires high frequency switches and polarity circuit requires low frequency switches. By lower number of MOSFET,s arrangement the power loss, conduction loss is decreased because when switch components are increased then switching loss and conduction loss increases. The alternative phase opposition deposition (APOD) strategy is selected for comparison. A multicarrier pulse wave modulated (MCPWM) level shifted scheme is used to control operation of power switches MOSFETS for multilevellevel cascaded multilevel H-bridge inverter CHMLI topology. The results of hardware and simulation are compared in term of improved efficiency, decreased switching and conduction loss, and lesser voltage stress dV/dt. The results have high power quality and better reduced electromagnetic interference.

Keywords: Voltage stress, Conduction loss, Efficiency, Power, Frequency, Boost converter

I. INTRODUCTION

Conventional inverter has been used since the past decades in the field of industrial applications and power systems of lower power usage[1]. Problems occurs when it comes to high power and high frequency usage[2]. Conventional inverters gives results that is not fulfils the requirement of voltage usage due to the incapable of reducing harmonic contents. It has high switching losses, lower efficiency and the lifespan of the systems due to long term constraining[3]. This requires to the growth of Multilevel Inverter (MLI), the creation of multiple DC levels that combined into sinusoidal wave which reduces harmonic distortion and increase efficiency[5]. MLI topologies are introduced to be functioning under high frequency with lesser switching losses and higher efficiency [6]. Therefore, a 9-level multilevel inverter is designed and simulated to produces a lower THD content[7]. Basic inverter circuits produces a square wave output with a certain degree of harmonics which is not helpful for the system applying inverter . This is why a nine multi-level inverter topology on hardware and simulation has been compared with 13 level in this paper which overcomes many weaknesses of normal inverter systems[7]. Multi-level inverters reduce the THD effectively as a result enhances the quality of the output voltage and produces reduced common mode voltage, which lowers switching losses and increase efficiency, while drawing current with minimal distortion. Optocouplers are used whose main task is to provide the pulse delay to MOSFETs which produces delay in levels of output[8]. In simulation same pulse angle is applied that is applied on hardware through Arduino code. A more bi-directional switches is added in the conventional H-Bridge to get additional voltage levels via a capacitor from a single DC voltage source, and final output is a stepped nine-level output voltage [11–17]. A

series and parallel connection of DC voltage sources cascaded with a conventional H-Bridge gives a stepped output with the reduced harmonics content in the output voltage [18,19]. It is proved in this paper that by increasing the number of levels the efficiency increases and THD decreases [20]. The outputs of each of different level H-bridge inverters are connected in series such that the synthesised waveform is almost a sinusoidal. Therefore the output has less harmonic distortion and switching losses are less compared to other inverter topologies [21].

II. INVERTER SYSTEM MODEL

The block diagram of INVERTER SYSTEM MODEL is shown in figure 1. The method used is hybrid multilevel circuits which separates the model in two parts i.e one is polarity circuit which generates polarity of circuit, the other is control circuit, that generates levels depending on the number of switches. The switches used in control circuit should have high switching frequency so it can generate required levels. The control circuit controls the output of inverter depending on input voltage and switching frequency. Each DC sources is connected with single H-bridge converter and AC terminal voltages of every level circuit are connected in series and can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero[9]. Output waveform is sum of individual inverter circuit. Cascaded multilevel inverter uses unique and attractive topology that is simple in structure, use less-number of components etc[10]. Their main advantage is that they can generate output voltages with extremely low distortion and lower voltage stress $\frac{dV}{dt}$.

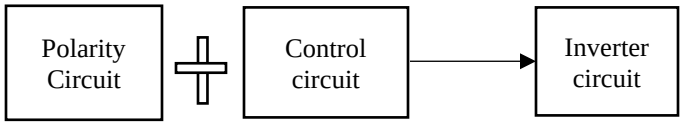

Figure 1. Hardware implementation of multilevel inverter.

III. HARDWARE IMPLEMENTATION ON HARDWARE

The 9 level inverter is designed on breadboard by using MOSFET,s switches. 9 level inverter is DC/AC inverter that generates 9 levels in output, the width of level depends on delay time set in microseconds. The hardware circuit is shown in Figure 2 and 3. This hardware is controlled by program run in Arduino. Optocouplers are used after capacitors to isolate output from input and get signal from Arduino. Arduino is used to apply the signal to MOSFET,s. MOSFET,s are switches that become ON by some gate pulse. Levels are introduce by adding some delay through Arduino coding. The phase relationship used is alternative phase opposition deposition (APOD) technique in which all carrier signal above zero are out of phase by 180º with signals which are below zero. Control circuit has four switches and polarity circuit has also four switches. The arrangement of switches is designed in IPD strategy to produce the inverter levels. The control circuit has four P-MOSFET,s and polarity circuit has two P-MOSFET, s and two N-MOSFET,s.

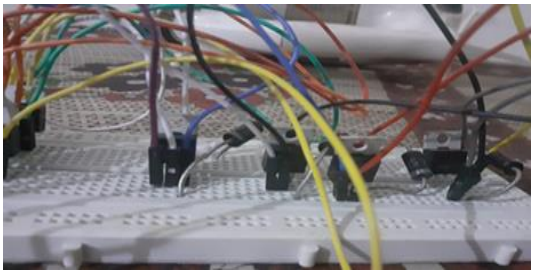

Figure 2. Control circuit

Figure 3. Polarity circuit

A. SWITCHING STATES OF MOSFET,S

The switching states of MOSFET,s are given in table 1.

S1	S2	S3	S4	S5	S6	S7	S8	S9	0	1	2	3	4	5	6
1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1
0	0	0	1	1	1	0	0	0	1	0	0	1	1	1	0
0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	0	1	1	0	0	0	0	0
0	1	1	1	1	1	1	1	0	1	1	0	0	0	0	0

Table 1 Switching states of MOSFET,s

By reverting polarity of switches in code we can invert the output voltage[10]. We can replace 1 with 0 to invert the value of voltage. From table 1 each switch has unique code. At every switch there must be switch which invert its pulse by itself. The 9 level inverter waveform can be displayed on oscilloscope in figure 4. The output resistance should be very low so we can achieve high efficiency.

Figure 4. Output of nine level inverter on Oscilloscope

As lower number of switches are added so switching loss is decreased. It can be seen from above figure that there is no distortion in output waveform the output has smooth level that's why $\frac{dV}{dt}$ will be low. The hardware circuit for 13 level inverter is shown in figure 5.

Figure 5. 13 level inverter hardware

13 level inverter has six P-MOSFET,s in control circuits that generates 6 plus levels and 6 negative levels and one zero level. For 13 level inverter six batteries are connected in series and MOSFET,s are controlled by Arduino through Optocoupler. The delay signal is added between different levels through Arduino code. Polarity circuit produce reverse polarity because it has two NPN and two PNP switches. Due to 13 level its efficiency is greater than 9 level inverter. The 13 level uses L-topolgy not H bridge because all switches are L series shape and parallel with polarity cicuit. The switching loss is calculated across V_{CE} and $R_{ON.}$The output of 13 level inverter is shown in figure 6.

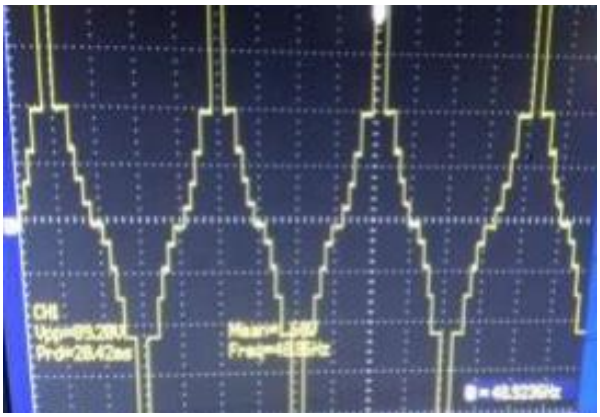

Figure 6. 13 level hardware output

In sine wave there is too much change in output voltage in short time so common mode voltage is high in pure sine wave but it is low in multilevel inverter due to stay in levels, because level stays constant for some time.

B. HARDWARE PARAMETERS

The input is applied which is DC and our required output frequency should be 50 Hz so the time period is 0.02. If we use higher frequency time period becomes less due to which delay become less. We have 16 patterns for our switches. For 9 level inverter we can calculate delay in this way. If T_p is time period and P_s is switching pattern then delay D is found by this formula.

$$D = \frac{T_p}{P_s}$$

Delay= $\frac{0.02}{16}$=0.00104=1.25ms (1)

So delay of 1.25ms will be added in every level.

Four batteries are used for input, each battery has voltage of 9V.

So total voltage is

$V_T=V_1+V_2+V_3+V_4$

As

$V_1=V_2=V_3=V_4=V$

So V_T=4V=4(9)

Input voltage= V_{in}= 36V

The input current is measured by DMM is,

Input current= I_{in} =0.016

Output voltage= V_o =1.59

Output resistance=R_L =10 ohm

From above information we can use these formulas

$$P_{in}=V_{in}\times I_{in} \quad (2)$$

Input power=36*.01=0.36

$$P_o = \frac{V_o^2}{R_L} \quad (3)$$

Output power=1.67^2/10=0.2788

$$\eta = \frac{P_o}{P_{in}}$$

(4)

Efficiency=0.2788/0.36=0.7747
Efficiency=0.7747×100=77.47 %
The total number of bidirectional switches in both control and polarity circuit are equal.
$N_c=N_p=n$
Now for 13 level inverter we can calculate efficiency,
Input current= I_{in} =0.017
Input Voltage= V_{in} =51.4
Output current= I_o =0.015
Output voltage= V_o =49.1

The efficiency for 13 level can be calculated as given formula

$$\eta = \frac{V_o I_o}{V_{in} I_{in}} \quad (5)$$

The efficiency is 84.29 % that is greater than 9 level inverter. The maximum and minimum voltage generated at output is given as

$$V_O = \sum_{k=1}^{n} \mathrm{V_{P_k}} + \sum_{k=1}^{n} \mathrm{V_{N_k}} \quad (5)$$

Where V_p and V_N are positive and negative voltage levels respectively.

C. SWITCHING LOSS AND CONDUCTION LOSS

In APOD in all modes of operations only two switches are in ON state so power loss is less than conventional H-bridge inverter.
If conduction loss during ON period is CL_{ON} then it can be expressed as

$$CL_{ON} = 2I_{CE}^2 R_{ON} \quad (6)$$

Where R_{ON} is conduction resistance in the switches and I_{CE} is forward current in collector and emitter terminals.
As in control circuit and polarity circuit operate in a way that polarity of voltage is inverted for every level hence switching loss SL_{SW} for switches is given as

$$SL_{SW} = f_s . C_{sw}(n+1)V_{OP} \quad (7)$$

Where f_s is switching frequency and C_{sw} is switching capacitance across emitter and collector of MOSFET. And V_{OP} is output peak voltage

IV. SIMULATION OF MULTI LEVEL INVERTER

Same parameters are used in simulation and the efficiency in simulation comes 96.76% in 9 Level and 98.02 % in 13 level. By using higher switching frequency, the time period become more less and delay has lower value. Figure 7 shows the control circuit in simulation which has four switches that are operated on same delay time.
The duty cycle in simulation can be added by this formula;
If phase delay is P_d and time period is T_p. Then Duty cycle D_c has been introduced by this formula

$$D_C = \frac{T_P - P_D}{T_P^2} \quad (8)$$

Formula can be justified by abbreviations given below

$$Duty\ cycle = \frac{time\ period - phase\ delay}{time\ period * time\ period}$$

All pulse generators are working on this formula but the difference is that the trigging angle is changed by multiple of odd integer.

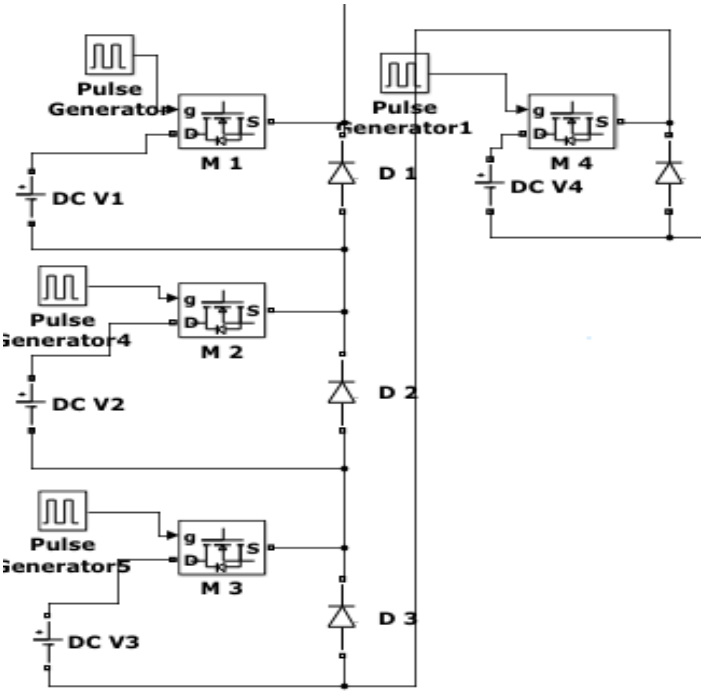

Figure 7. Control circuit of simulation

Figure 8 shows polarity circuit with two MOSFET,s that are triggered by same pulse generator parameters to produce positive polarity and other two triggered through same pulse generator to produce negative polarity as shown in figure 6.

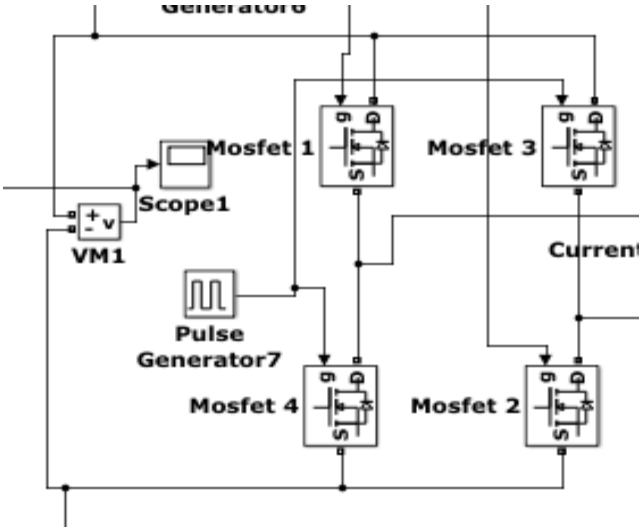

Figure 8. Polarity circuit of simulation

Figure 9 shows the efficiency calculation diagram in which input current and voltage are multiplied to get input power and output current and output voltage are multiplied to get output power. The efficiency is improved upto 96.76 %.

Then output power is divided to input power to get efficiency. As shown in figure 9 the voltage and current are multiplied to get power of input and output. Then efficiency is calculated by dividing output power to input power.

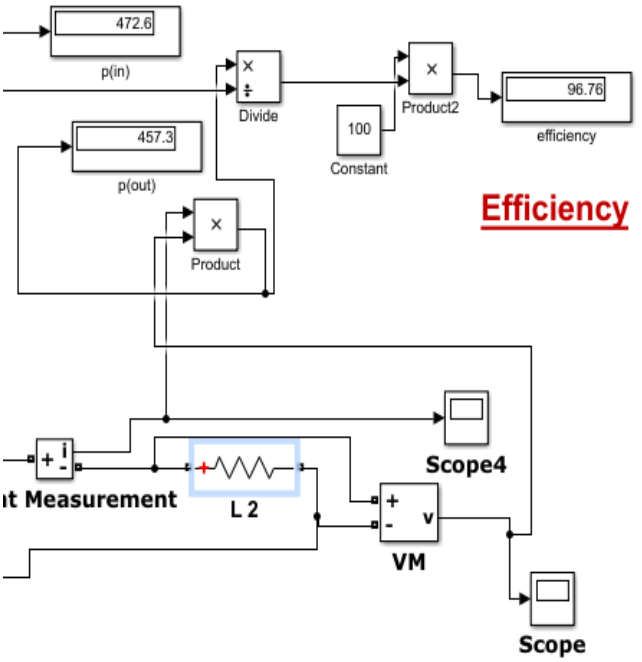

Figure 9. Efficiency calculation on Simulink

The output of 9 Levels can be examine on scope in figure 10 where 9 levels are clearly shown and every level stays constant for some duration of time.
In figure 10 it is clearly shown that the output voltage in each level stays constant for some duration of time which lowers the $\frac{dV}{dt}$, which results decreases the common mode voltage stress .

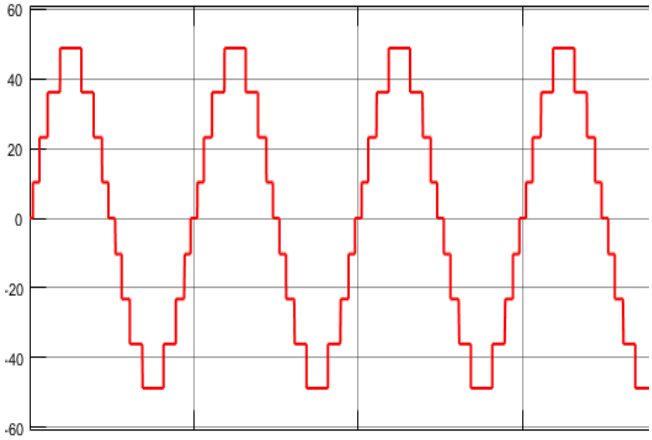

Figure 10. 9 level inverter output

Time harmonic distortion is the ratio of sum of all power of all the harmonic components to the power of fundamental frequency component, As fundamental frequency power is higher due to low switching and conduction loss hence THD decrease to 10.98 %. In previous papers THD was improved upto 14.18 % but in this paper it has been reduced upto 10.98 % as shown in figure 11.

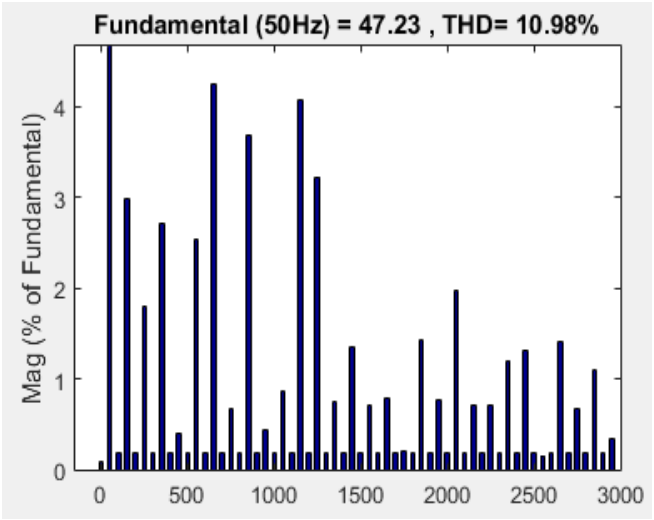

Figure 11. THD analysis

Now for 13 Level simulation, the control circuit is shown in figure 12, The control circuit has six MOSFET,s switches and these are connected in L shape. The signal is applied by high

switching frequency and pulse is applied at MOSFET,s through pulse generator.

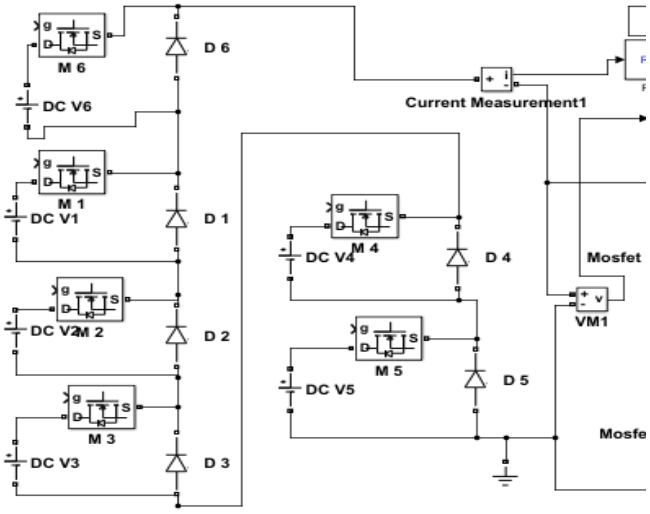

Figure 12. Thirteen level control circuit

The switching loss can be calculated through current between collector and emitter. Due to high value capacitors, the I_{CE} is low and we already know R_{ON} is also low. So product of I_{CE} and R_{ON} is very low. The polarity circuit with efficiency calculations circuit is describe in figure 13

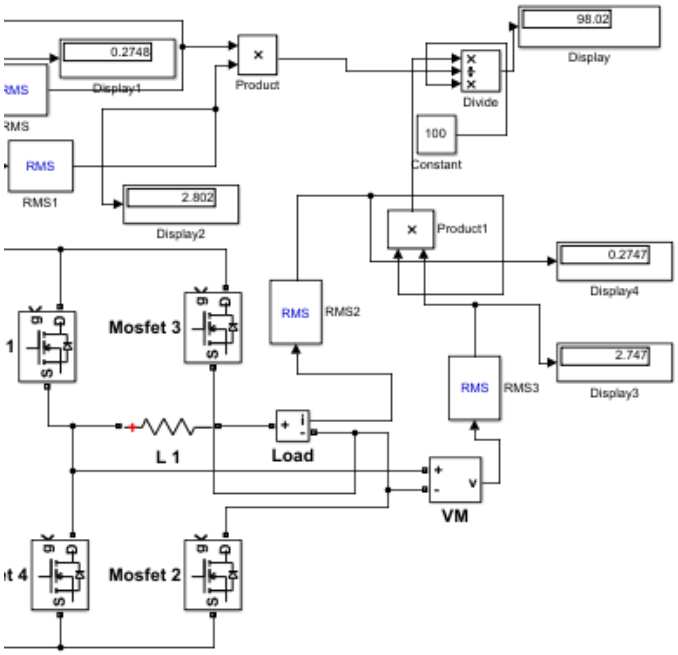

Figure 13. Thirteen level inverter efficiency

THD for 13 level is reduced to 9.97 % that is also greater than THD in 9 level inverter which is 10.48 %. THD for 13 level Is shown in figure 14.

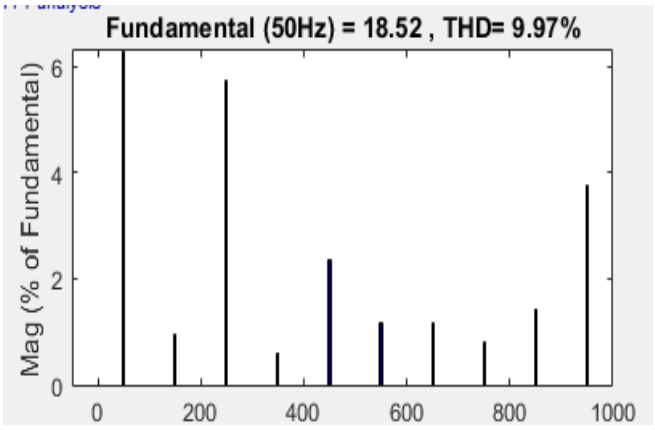

Figure 14. Time harmonic distortion in 13 level inverter

Form above comparison it is cleared that by increasing level the efficiency is increased and THD becomes low.

V. CONCLUSION

As from simulation and hardware results it is clear that using higher frequency, high value capacitors and lower number of components increases the efficiency. As voltage remains constant for small duration of time period so there is no change in voltage which lowers the value of $\frac{dV}{dt}$. As dV is small for small duration of time which lowers voltage stress. The THD has been decreased upto 10.98% in 9 Level and 9.97% in 13 Level inverter. Due to less number of switches and less connection of wires the switching loss and conduction loss decreases. Switching loss decreases because R_{ON} is less and conduction loss is less because of higher capacitance. The efficiency in hardware of 9 level is 77.47 % and in 13 level 84.29 % and in simulation it increases upto 96.76 % in 9 level and 98.02 % in 13 level. So lower number of switches and lower number of connections, the losses are decreased. By using new formula for trigging angle efficiency becomes higher than previous results. The switching loss can be further decreased by high value capacitors and in Boost inverters. Due to APOD technique which uses 0- and 180-degree arrangements the inverter becomes more efficient. The electromagnetic interference can be reduced by ensuring the ground level and twisting the DC side cables, this will eliminate radiated noise from switches.

FUTURE WORK

The given work can be extended by using soft switching technique in which there is no conduction loss and switching loss. ZVS technique greatly reduce the THD and voltage stress. The Electromagnetic interference at very high switching frequency becomes very high which also can be eliminated by soft switching.

VI. REFERENCES

[1] M. Islam and S. Mekhilef, "Efficient transformerless mosfet inverter for a grid-tied photovoltaic system," IEEE Trans. on Power Electronics, vol. 31, no. 9, pp. 6305–6316, 2016.

[2] Rathore S.; Kirar M. K.; S.K Bhardwaj, Simulation of Cascaded H-Bridge Multilevel Inverter using PD, POD, APOD Techniques. Electrical & Computer Engineering: An international Joinal (ECIJ) Volume 4, No. 3. September 2015.

[3] Rajesh Ingale. Harmonic Analysis Using FFT and STFT. International Journal of Signal Processing and Pattern Recognition, Vol. 7, No. 4. 2014.

[4] Amarendra Edpuganti and Akshay K. Rathore 2015 Optimal Low Switching Frequency Pulse width Modulation of Nine-Level Cascade Inverter IEEE Transactions on Power Electronics 30, pp -482 – 495.

[5] Mohd Ruddin Ab Ghani, Nabil Farah, Jurifa Lazi. Investigation Study of Three-Level Cascaded H-Bridge Multilevel Inverter. TELKOMNIKA. 2017; 15(1): 125-137.

[6] Kokate, M. N., Comparison of Simulation Results Three Level and Five Level H-Bridge Inverter and Hardware Implementation of Single Leg H-Bridge Three Level Inverter. International Journal of Innovative Research & Studies (ISSN 2319-9725). Nagpur, India. April, 2013.

[7] Z. Moradi-Shahrbabak, A. Tabesh, and G. R. Yousefi, "Economical Design of Utility-Scale Photovoltaic Power Plants With Optimum Availability," IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3399–3406, Jul. 2014.

[8] A. Sangwongwanich, Y. Yang, F. Blaabjerg, and D. Sera, "Delta Power Control Strategy for Multistring Grid-Connected PV Inverters," IEEE Trans. Ind. Appl., vol. 53, no. 4, pp. 3862–3870, Jul. 2017.

[9] C. D. Fuentes, C. A. Rojas, H. Renaudineau, S. Kouro, M. A. Perez, and T. Meynard, "Experimental Validation of a Single DC Bus Cascaded H-Bridge Multilevel Inverter for Multistring Photovoltaic Systems," IEEE Trans. Ind. Electron., vol. 64, no. 2, pp. 930–934, Feb. 2017.

[10] Haddadi, A. M., Farhangi, S., & Blaabjerg, F. (2018). A Reliable Three-Phase Single-Stage Multi-Port Inverter for Grid-Connected Photovoltaic Applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

[11]. Park, S.J.; Kang, F.S.; Lee, M.H.; Kim, C.U. A new single-phase five level PWM inverter employing a deadbeat control scheme. IEEE Trans. Power Electron. 2003, 18, 831–843.

[12]. Selvaraj, J.; Rahim, N.A. Multilevel inverter for grid-connected PV system employing digital PI controller. IEEE Trans. Ind. Electron. 2009, 56, 149–158.

[13. Cegli, G.; Guzman, V.; Sanchez, C.; Ibanez, F.; Walter, J.; Gimaez, M.I. A new simplified multilevel inverter topology for DC–AC conversion. IEEE Trans. Power Electron. 2006, 21, 1311–1319.

[14]. Martins, G.M.; Pomilio, J.A.; Buso, S.; Spiazzi, G. Three-phase low frequency commutation inverter for renewable energy systems. IEEE Trans. Ind. Electron. 2006, 53, 1522–1528.

[15]. Rahim, N.A.; Chaniago, K.; Selvaraj, J. Single-Phase Seven-Level Grid-Connected Inverter for Photovoltaic System. IEEE Trans. Ind. Electron. 2011, 58, 2435–2443.

[16]. Shanmugavadivu, N.; Annamalai, T. Single Phase Seven Level Stand Alone Inverter for Photovoltaic System. Bonfring Int. J. Power Syst. Integr. Circuits 2012, 2, 49–53.

[17]. Hinago, Y.; Koizumi, H. A single phase multilevel inverter using switched series/parallel DC voltage sources.In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE 2009), San Jose, CA, USA, 20–24 September 2009; pp. 1962–1967.

[18].Hinago, Y.; Koizumi, H. A Single-Phase Multilevel Inverter Using Switched Series/Parallel DC Voltage Sources. IEEE Trans. Ind. Electron. 2010, 57, 2643–2650.

[19] Cheng Y, Qian C, Crow ML, et al. (2006) A Comparison of Diode-Clamped and Cascaded Multilevel Converters for a STATCOM with Energy Storage. IEEE T Ind Electron 53: 1512-1521.

[20] Muhammad Usman Javed, Safdar Raza, & Muhammad Ali. (2020). Fault current analysis and its effects comparison on HVDC and HVAC of 660kV Matiari to Lahore project (Pakistan). *University of Sindh Journal of Information and Communication Technology* , *4*(3), 109-114. Retrieved from.

[21] Nouman Naseem, Azka Arif, Shahzaib Ahmed, Dr. Sarwat Nizamani, Salman Khawaja, & Abdul Samad Jamali. (2020). Electronic Toll Collection and Record Management System. *University of Sindh Journal of Information and Communication Technology* , *4*(3), 129 - 133. Retrieved from https://sujo.usindh.edu.pk/index.php/USJICT/article/view/2877